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MS-7613 Ver: 11 uATX(244mm X 244mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:SLI SL28748ELC-T

HD Audio Codec:ALC888S

LAN:RTL8111DL 10/100/1000

IO: Fintek F71858D

Flash ROM: 32 Mb SPI (CHIP) Fire wire: VIA VT6315N

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

Mini PCI Express (X1) Slot * 1

ONFI Slot *1

PWM:

Controller:Intersil ISL6333 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *6

USB2.0 *14 (Rear*6 / Front*8)

on BOARD BUZZER

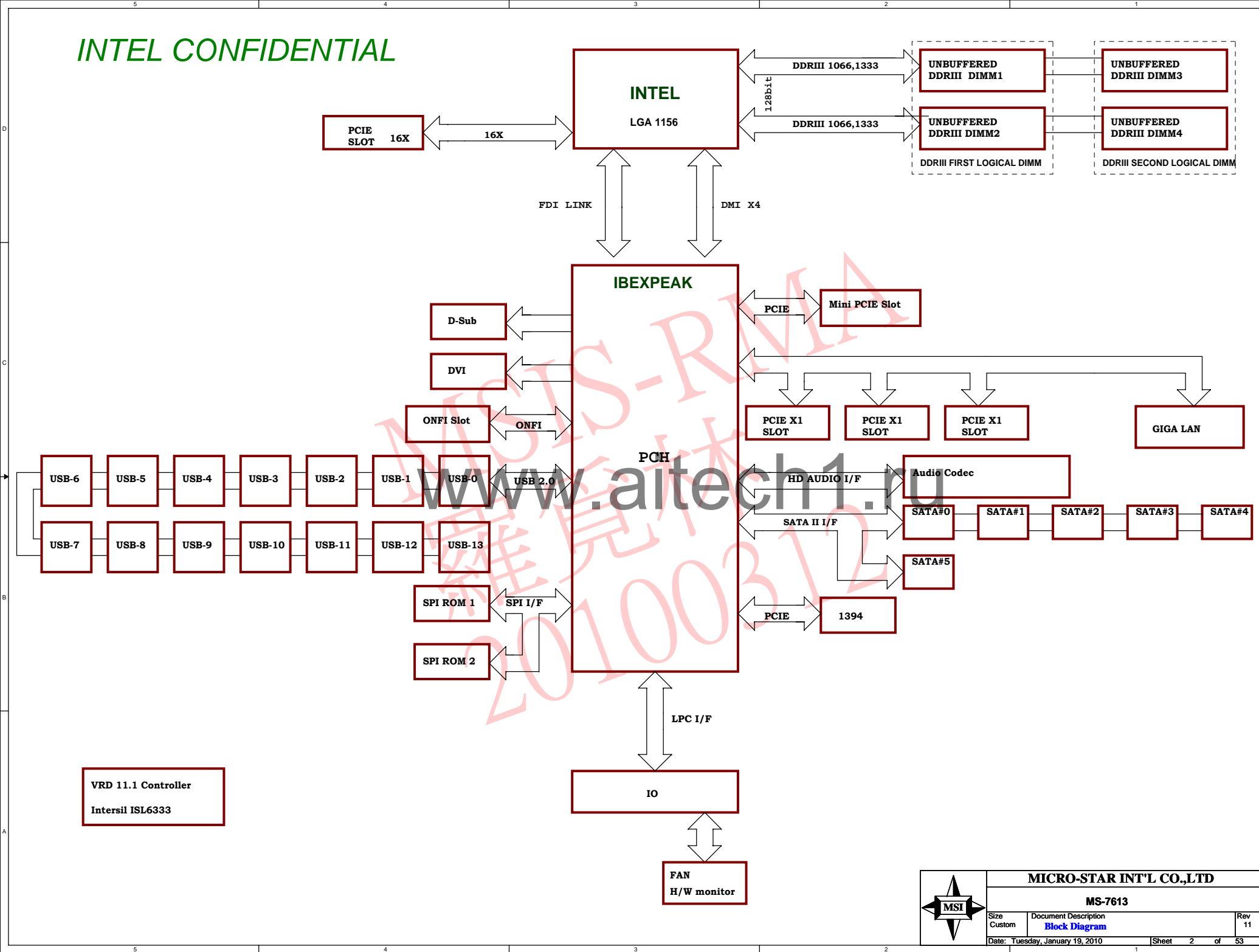
D-SUB *1

DVI PORT*1



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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9↓
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #3	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes



				18BXPSAK GPIO DEFINITION	
GPIO	POWER	IO	Function	Implementation	Mother board Function
GPIO0	MAIN	1	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	1	TACH1	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	1	PCLIRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	1	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMMM 8 assembly connects pin 12 directly to GND	COMM_8_DET#/ MOM_TH_ALRT#
GPIO7	MAIN	1	TACH3	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUMB	0	ICG_B#		Reserved
GPIO9	RESUMB	1	OC5	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUMB	1	OC6	10K Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#
GPIO11	RESUMB	1	SMBALERT#	20K Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUMB	1	LAN_DISABLE	Follow implementation in Intel Picton Design Guide	LAN_DISABLE#
GPIO13	RESUMB	1	IO_PMB	10K Pull-up to +3.3V and connect to P151-pin 10; also add a no-installed pull-down to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUMB	1	OC7	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUMB	1	PCB_GPIO15		Reserved
GPIO16	RESUMB	0	SATA2DP	10 M pull-up to VBAT and connect to CPU SKT0CC#, SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	1	TACH0	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	1	PCIECLKRQ#	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	1	SATA1DP	connect to a test point	unused
GPIO20	MAIN	1	PCIECLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKRQ2#
GPIO21	MAIN	1	SATA2DP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	1	SCLOCK	10K Pull-up to +3.3V and connect to P160-pin 10	INT_USB_DET#
GPIO23	MAIN	1	LDRO#	connect to a test point.	PEG_MOM_DET#
GPIO24	RESUMB	0	MBALED	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ3#
GPIO26	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ4#
GPIO27	RESUMB	0	OD_PLL_VR_EN	10K pull-up to +3.3VAUX	Reserved
GPIO28	RESUMB	0	PCB_GP28	connect to a test point	unused
GPIO29	RESUMB	0	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUMB	1	SUS_PWRACK	100K Pull-up to 3V_AUX	unused
GPIO31	MAIN	1	ACPRESENT	10K Pull-up to +3.3V and connect to P25-pin 10	FRONT_USB_DET1#
GPIO32	MAIN	0	PCB_GP32	Through a 1kΩ series resistor, 10K pull-up to +3.3V and connect to P2-pin 6.	NON-EPA_PS_DET#

GPIO33	MAIN	0	PCB_GP33	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	0	SP_PC#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-up to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	0	SATACLKRQ#	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	1	SATA2DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	1	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	1	SLOAD	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUMB	1	OC1	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for XDP implementation. 8.2kΩ pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUMB	1	OC2	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUMB	1	OC3	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUMB	1	OC4	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKRQ6#
GPIO45	RESUMB	1	PCIECLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J3-pin8 I7	PRSN#_J31
GPIO46	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ7#
GPIO47	RESUMB	1	PBG_A_CLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J4-pin848 and B81	PRSN#_J41
GPIO48	MAIN	1	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	0	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	1	PCLRBQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	0	PCLQNT#1	connect to a test point	GNT1#
GPIO52	MAIN	1	PCLRBQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	0	PCLQNT#2	connect to a test point	GNT2#
GPIO54	MAIN	1	PCLRBQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14-pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	0	PCLQNT#3	connect to a test point	GNT3#
GPIO56	RESUMB	1	PBG_B_CLKRQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	1	PCB_GP57	10K Pull-up to +3.3VME installed and 10K pull-down to GND not installed.	TPM_PP

GPIO58	RESUMB	0	SMCLK	10K pull-up to 3V_AUX	SMCLK
GPIO59	RESUMB	1	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALARM
GPIO61	RESUMB	0	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUMB	0	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUMB	0	SLP_S#	Connect to the SIO-pin37	SLP_S#
GPIO64	MAIN	0	CLKOUTFLBK0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK0
GPIO65	MAIN	0	CLKOUTFLBK1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK1
GPIO66	MAIN	0	CLKOUTFLBK2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK2
GPIO67	MAIN	0	CLKOUTFLBK3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUMB	1	PCB_GP72	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET0#
GPIO73	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3VAUX and through a 0Ω series resistor, connect to J42-pin8 I7, B31, B48, and B81	PRSN#_J42
GPIO74	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALERT#
GPIO75	RESUMB	0	SMDLIDATA	10K pull-up to 3V_AUX	SMDLIDATA



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CK505

PCICLK_LOOP

BCLK(133M)

DMI(100M) GEN2

SATA(100M)

DOT(96M)

REF(14.318M)

PCH

BCLK(133M)

DMI(100M) GEN2

PCIECLK(100M) GEN2

PCIECLK(100M) GEN2

PCIECLK(100M) GEN2

PCIECLK(100M) GEN2

PCIECLK(100M) GEN2

PCICLK(33M)

CPU

CPU

PCIE_X16 SLOT

PCIE_X1 SLOT

GBLAN

1394

Mini PCIE SLOT

SIO

14.318M XTAL



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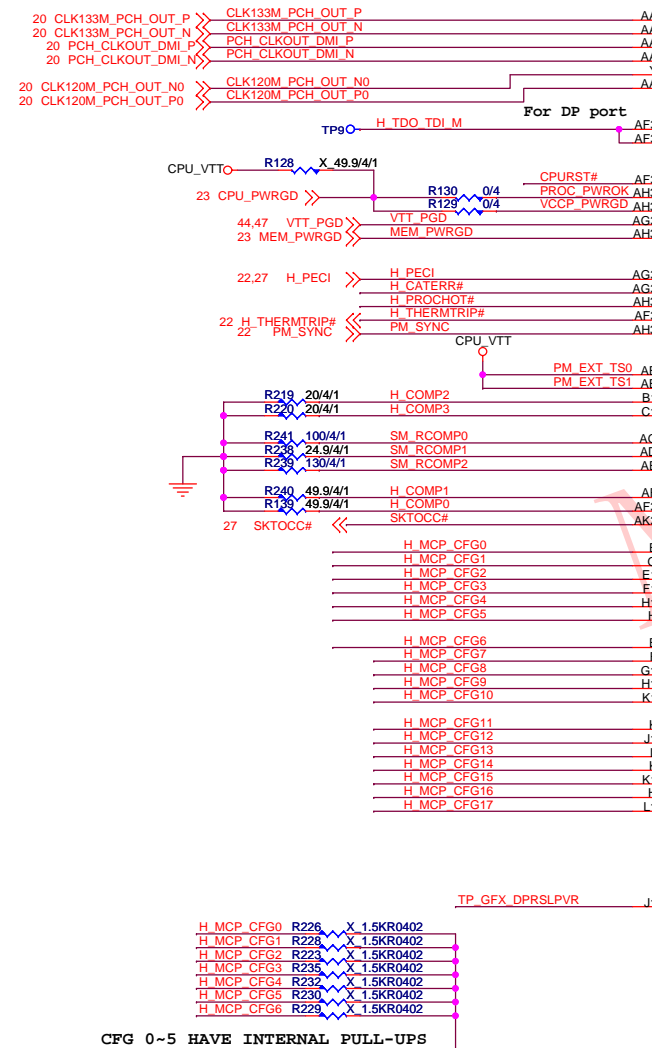
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Clock Distribution

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11

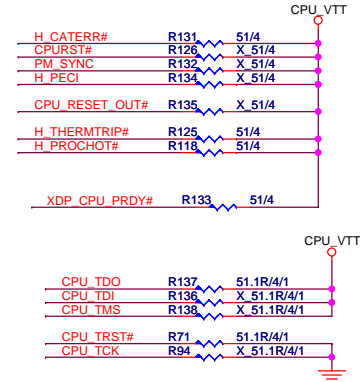
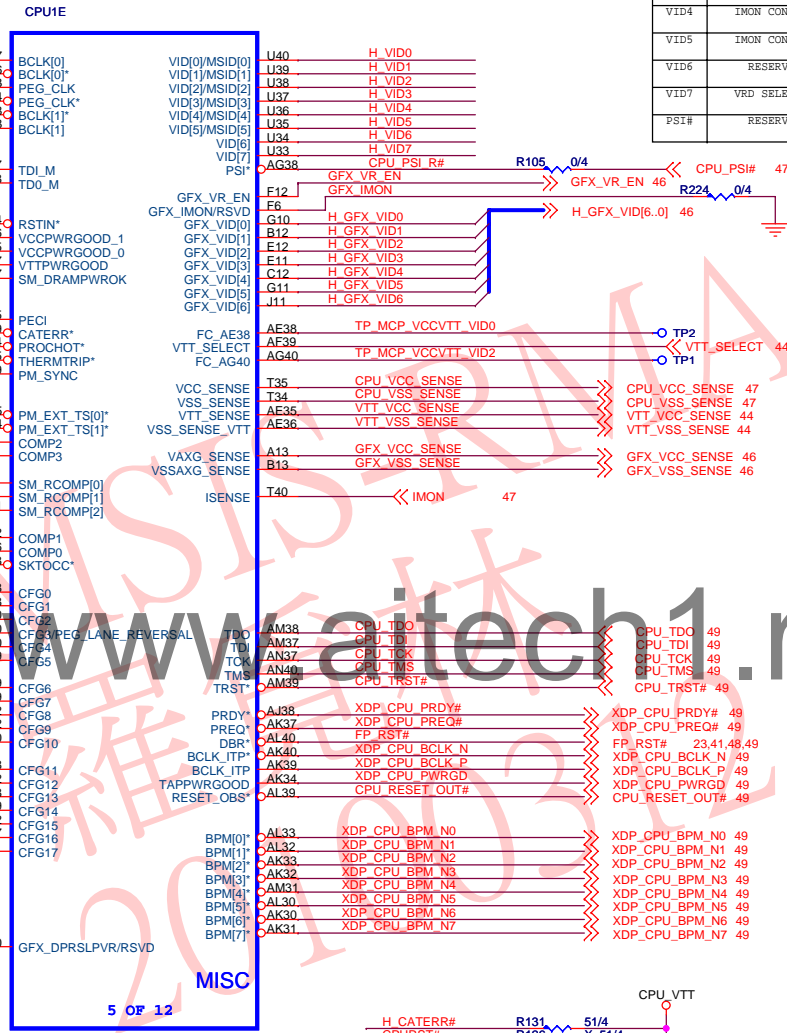
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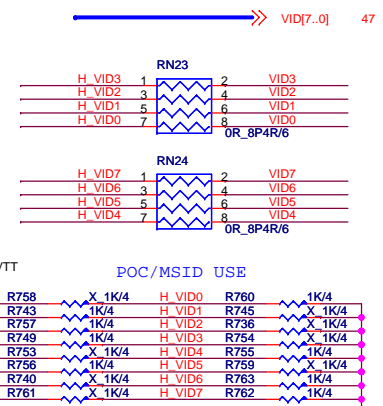


CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	SEE PEG CONFIG TABLE		PEG SEL1
2	SEE PEG CONFIG TABLE		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLED	DP PRESENCE
5			

PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

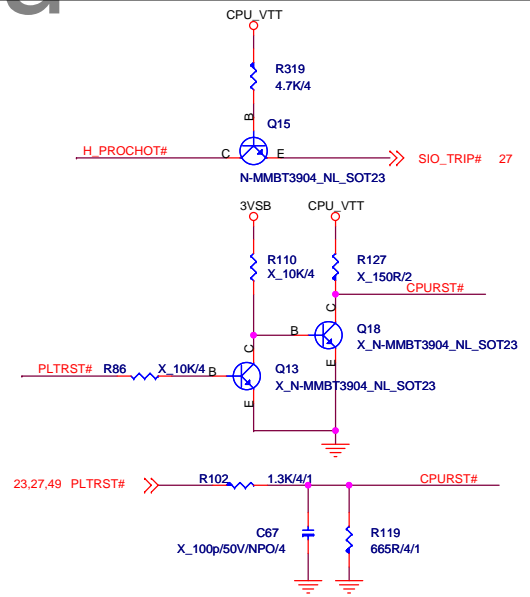


	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG2	1
VID6	RESERVED	
VID7	VBD SELECT	LOW
PSI#	RESERVED	LOW



Market Segment Selection Truth Table for MSI0[2:0]			
MSI2	MSI1	MSI0	Description ¹
1	1	0	Lynnfield and Havendale processors supported ³

Processor Icc(max)	I _{MAX}	POC Gain Setting
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111



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13,14 MEM_MA_DATA[63..0]

13,14 MEM_MA_ADD[15..0]

13,14 MEM_MA_WE_L
13,14 MEM_MA_CAS_L
13,14 MEM_MA_RAS_L

13,14 MEM_MA_BANK0
13,14 MEM_MA_BANK1
13,14 MEM_MA_BANK2

13 MEM_MA_CS_L0
13 MEM_MA_CS_L1
14 MEM_MA_CS_L2
14 MEM_MA_CS_L3

13 MEM_MA_CKE0
13 MEM_MA_CKE1
14 MEM_MA_CKE2
14 MEM_MA_CKE3

13 MEM_MA_ODT0
13 MEM_MA_ODT1
14 MEM_MA_ODT2
14 MEM_MA_ODT3

13 MEM_MA_CLK_H0
13 MEM_MA_CLK_L0
13 MEM_MA_CLK_H1
14 MEM_MA_CLK_L1
14 MEM_MA_CLK_H2
14 MEM_MA_CLK_L2
14 MEM_MA_CLK_H3
14 MEM_MA_CLK_L3

13,14,15,16 DDR3_DRAMRST#

CPU1A

SA_MA[0]
SA_MA[1]
SA_MA[2]
SA_MA[3]
SA_MA[4]
SA_MA[5]
SA_MA[6]
SA_MA[7]
SA_MA[8]
SA_MA[9]
SA_MA[10]
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SA_MA[12]
SA_MA[13]
SA_MA[14]
SA_MA[15]

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SA_CAS*
SA_RAS*

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SA_BA[1]
SA_BA[2]

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SA_CS[1]*
SA_CS[2]*
SA_CS[3]*

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SA_CK[2]
SA_CK[2]*
SA_CK[3]
SA_CK[3]*

SM_DRAMRST*

SA_CS[4]*
SA_CS[5]*
SA_CS[6]*
SA_CS[7]*

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SA_DQS[8]*

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SA_ECC_CB[7]

DDR_A

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SA_DQ[63]

AK3 MEM_MA_DQS_H0
AJ3 MEM_MA_DQS_L0
AJ2 MEM_MA_DM0

AH1 MEM_MA_DATA0
AJ4 MEM_MA_DATA1
AL2 MEM_MA_DATA2
AL1 MEM_MA_DATA3
AG2 MEM_MA_DATA4
AH2 MEM_MA_DATA5
AK1 MEM_MA_DATA6
AK2 MEM_MA_DATA7

AP2 MEM_MA_DQS_H1
AP3 MEM_MA_DQS_L1
AN1 MEM_MA_DM1

AN3 MEM_MA_DATA8
AN2 MEM_MA_DATA9
AR3 MEM_MA_DATA10
AR2 MEM_MA_DATA11
AM3 MEM_MA_DATA12
AM2 MEM_MA_DATA13
AP1 MEM_MA_DATA14
AR4 MEM_MA_DATA15

AL4 MEM_MA_DQS_H2
AL3 MEM_MA_DQS_L2
AU1 MEM_MA_DM2

AT4 MEM_MA_DATA16
AU2 MEM_MA_DATA17
AU3 MEM_MA_DATA18
AU4 MEM_MA_DATA19
AT3 MEM_MA_DATA20
AT1 MEM_MA_DATA21
AV2 MEM_MA_DATA22
AV4 MEM_MA_DATA23

AV6 MEM_MA_DQS_H3
AV6 MEM_MA_DQS_L3
AV6 MEM_MA_DM3

AW5 MEM_MA_DATA24
AY5 MEM_MA_DATA25
AU8 MEM_MA_DATA26
AU8 MEM_MA_DATA27
AU8 MEM_MA_DATA28
AU5 MEM_MA_DATA29
AV7 MEM_MA_DATA30
AW7 MEM_MA_DATA31

AR28 MEM_MA_DQS_H4
AR28 MEM_MA_DQS_L4
AN28 MEM_MA_DM4

AN27 MEM_MA_DATA32
AT28 MEM_MA_DATA33
AP28 MEM_MA_DATA34
AP30 MEM_MA_DATA35
AN26 MEM_MA_DATA36
AR27 MEM_MA_DATA37
AR29 MEM_MA_DATA38
AN30 MEM_MA_DATA39

AV32 MEM_MA_DQS_H5
AV32 MEM_MA_DQS_L5
AV31 MEM_MA_DM5

AU30 MEM_MA_DATA40
AU31 MEM_MA_DATA41
AV33 MEM_MA_DATA42
AU34 MEM_MA_DATA43
AV30 MEM_MA_DATA44
AV30 MEM_MA_DATA45
AU33 MEM_MA_DATA46
AW33 MEM_MA_DATA47

AW36 MEM_MA_DQS_H6
AV35 MEM_MA_DQS_L6
AU35 MEM_MA_DM6

AW35 MEM_MA_DATA48
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AV37 MEM_MA_DATA50
AU37 MEM_MA_DATA51
AY34 MEM_MA_DATA52
AW34 MEM_MA_DATA53
AV36 MEM_MA_DATA54
AW37 MEM_MA_DATA55

AR39 MEM_MA_DQS_H7
AR38 MEM_MA_DQS_L7
AT38 MEM_MA_DM7

AT39 MEM_MA_DATA56
AT40 MEM_MA_DATA57
AN38 MEM_MA_DATA58
AN39 MEM_MA_DATA59
AU38 MEM_MA_DATA60
AU39 MEM_MA_DATA61
AP39 MEM_MA_DATA62
AP40 MEM_MA_DATA63

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15,16 MEM_MB_DATA[63..0]

15,16 MEM_MB_ADD[15..0]

CPU1B

15,16 MEM_MB_WE_L
15,16 MEM_MB_CAS_L
15,16 MEM_MB_RAS_L

15,16 MEM_MB_BANK0
15,16 MEM_MB_BANK1
15,16 MEM_MB_BANK2

15 MEM_MB_CS_L0
15 MEM_MB_CS_L1
16 MEM_MB_CS_L2
16 MEM_MB_CS_L3

15 MEM_MB_CKE0
15 MEM_MB_CKE1
16 MEM_MB_CKE2
16 MEM_MB_CKE3

15 MEM_MB_ODT0
15 MEM_MB_ODT1
16 MEM_MB_ODT2
16 MEM_MB_ODT3

15 MEM_MB_CLK_H0
15 MEM_MB_CLK_L0
15 MEM_MB_CLK_H1
15 MEM_MB_CLK_L1
16 MEM_MB_CLK_H2
16 MEM_MB_CLK_L2
16 MEM_MB_CLK_H3
16 MEM_MB_CLK_L3

MEM_MB_ADD0 AU20
MEM_MB_ADD1 AU18
MEM_MB_ADD2 AV18
MEM_MB_ADD3 AU17
MEM_MB_ADD4 AY18
MEM_MB_ADD5 AV17
MEM_MB_ADD6 AW17
MEM_MB_ADD7 AU16
MEM_MB_ADD8 AT17
MEM_MB_ADD9 AY16
MEM_MB_ADD10 AY25
MEM_MB_ADD11 AW16
MEM_MB_ADD12 AW15
MEM_MB_ADD13 AW28
MEM_MB_ADD14 AY12
MEM_MB_ADD15 AV11

MEM_MB_WE_L AU26
MEM_MB_CAS_L AW27
MEM_MB_RAS_L AW26

MEM_MB_BANK0 AU25
MEM_MB_BANK1 AW25
MEM_MB_BANK2 AV12

MEM_MB_CS_L0 AY27
MEM_MB_CS_L1 AW29
MEM_MB_CS_L2 AV26
MEM_MB_CS_L3 AV29

MEM_MB_CKE0 AW8
MEM_MB_CKE1 AY9
MEM_MB_CKE2 AU9
MEM_MB_CKE3 AV9

MEM_MB_ODT0 AU27
MEM_MB_ODT1 AU29
MEM_MB_ODT2 AW27
MEM_MB_ODT3 AU28

MEM_MB_CLK_H0 AR17
MEM_MB_CLK_L0 AR16
MEM_MB_CLK_H1 AT15
MEM_MB_CLK_L1 AR15
MEM_MB_CLK_H2 AN17
MEM_MB_CLK_L2 AN15
MEM_MB_CLK_H3 AR19
MEM_MB_CLK_L3 AR18

AM23
AM24
AL24
AK24

AR14
AR13

AR12
AT13
AN15
AP14
AM12
AN12
AN14
AP13

DDR_B

2 OF 12

SB_MA[0]
SB_MA[1]
SB_MA[2]
SB_MA[3]
SB_MA[4]
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SB_DQ[63]

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AE5 MEM_MB_DQS_L0
AE4 MEM_MB_DM0
AD7 MEM_MB_DATA0
AD6 MEM_MB_DATA1
AH8 MEM_MB_DATA2
AJ8 MEM_MB_DATA3
AC7 MEM_MB_DATA4
AC6 MEM_MB_DATA5
AE5 MEM_MB_DATA6
AE6 MEM_MB_DATA7
AH6 MEM_MB_DQS_H1
AJ5 MEM_MB_DQS_L1
AH4 MEM_MB_DM1
AG5 MEM_MB_DATA8
AH7 MEM_MB_DATA9
AK6 MEM_MB_DATA10
AL4 MEM_MB_DATA11
AG6 MEM_MB_DATA12
AG4 MEM_MB_DATA13
AJ7 MEM_MB_DATA14
AK7 MEM_MB_DATA15
AN6 MEM_MB_DQS_H2
AM6 MEM_MB_DQS_L2
AM7 MEM_MB_DM2
AL6 MEM_MB_DATA16
AN5 MEM_MB_DATA17
AP6 MEM_MB_DATA18
AR5 MEM_MB_DATA19
AL5 MEM_MB_DATA20
AM4 MEM_MB_DATA21
AN7 MEM_MB_DATA22
AP5 MEM_MB_DATA23
AR8 MEM_MB_DQS_H3
AP8 MEM_MB_DQS_L3
AT7 MEM_MB_DM3
AT6 MEM_MB_DATA24
AR7 MEM_MB_DATA25
AP9 MEM_MB_DATA26
AM8 MEM_MB_DATA27
AN8 MEM_MB_DATA28
AR6 MEM_MB_DATA29
AL8 MEM_MB_DATA30
AT9 MEM_MB_DATA31
AT25 MEM_MB_DQS_H4
AR24 MEM_MB_DQS_L4
AN24 MEM_MB_DM4
AN23 MEM_MB_DATA32
AP23 MEM_MB_DATA33
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AP26 MEM_MB_DATA35
AT23 MEM_MB_DATA36
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AT26 MEM_MB_DATA39
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AR31 MEM_MB_DATA45
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AT33 MEM_MB_DATA47
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AN34 MEM_MB_DATA54
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AJ36 MEM_MB_DATA58
AJ37 MEM_MB_DATA59
AN35 MEM_MB_DATA60
AM34 MEM_MB_DATA61
AJ35 MEM_MB_DATA62
AL36 MEM_MB_DATA63

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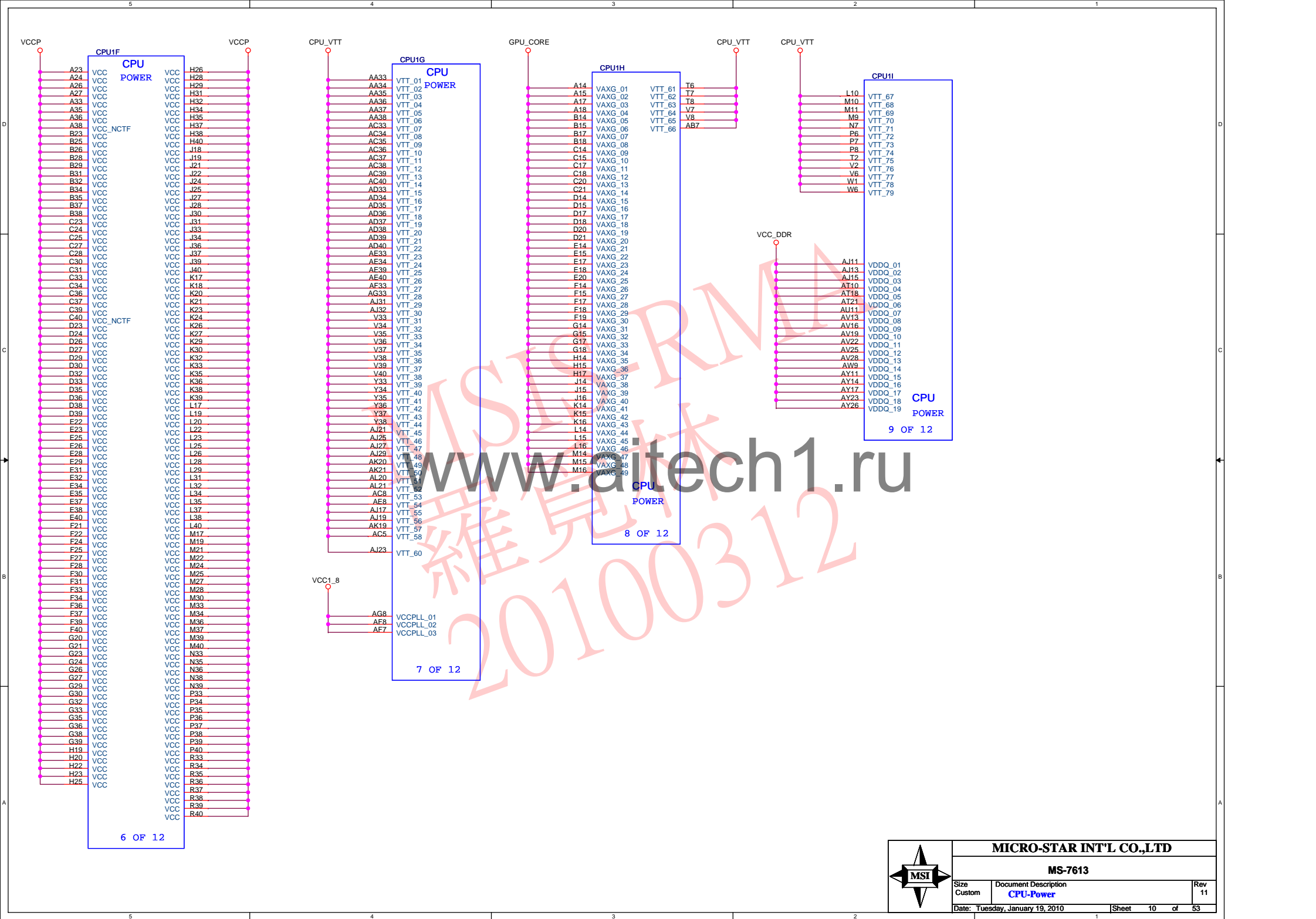


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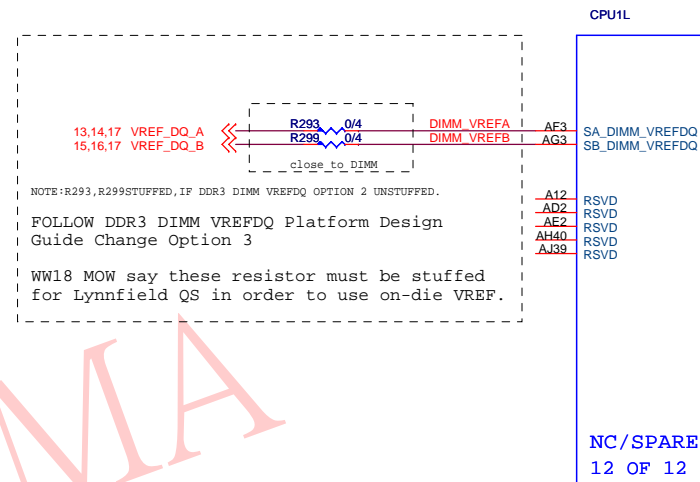
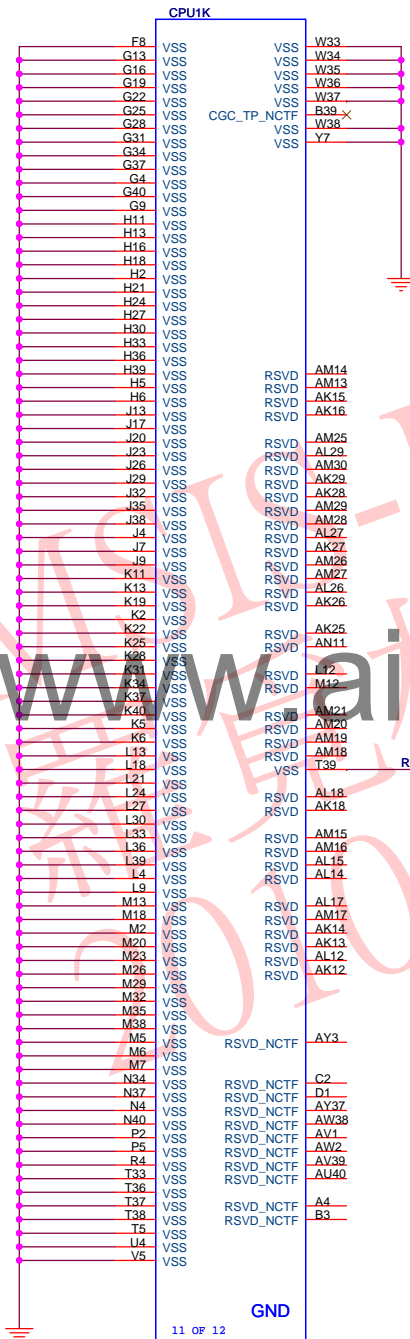
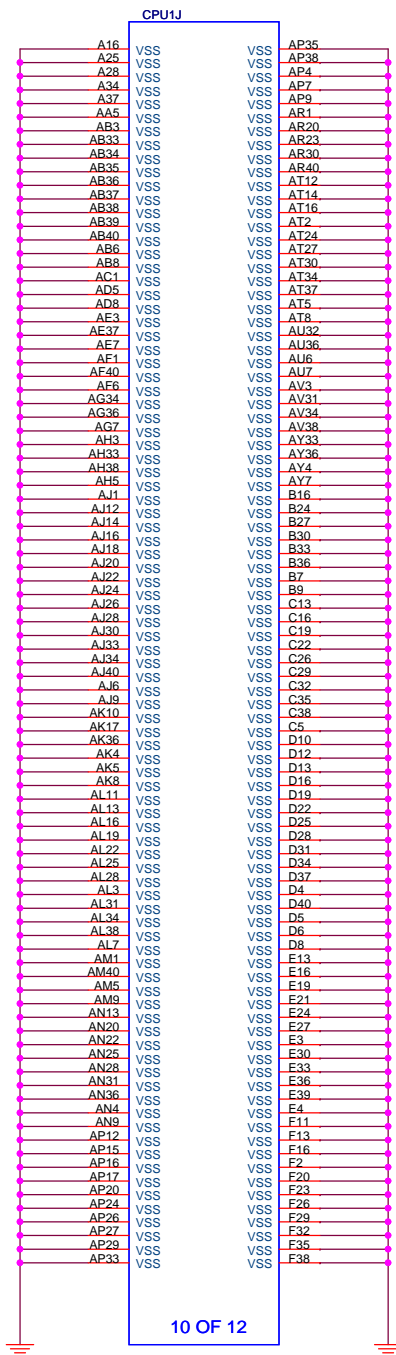
Date: Tuesday, January 19, 2010 Sheet 8 of 53



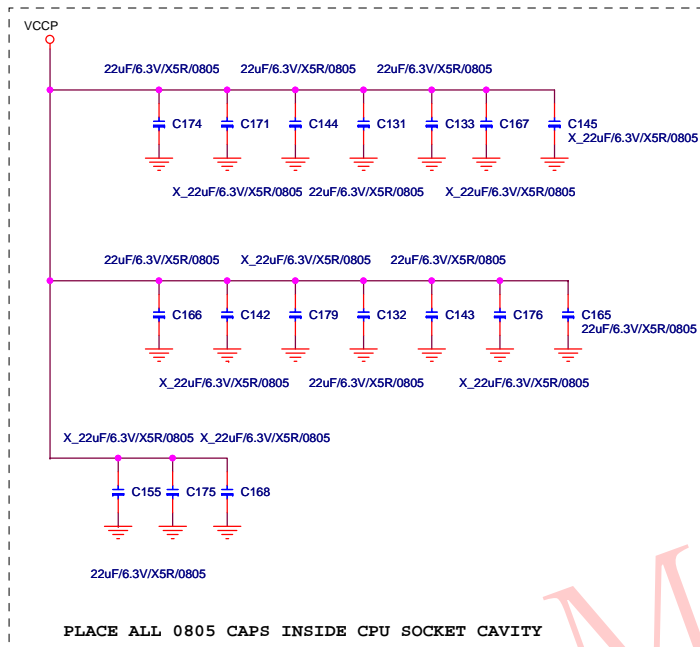
MICRO-STAR INT'L CO.,LTD

MS-7613

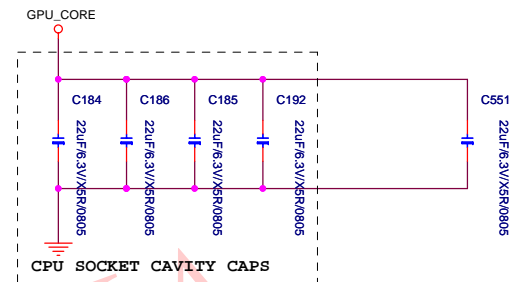
Size	Document Description	Rev
Custom	CPU-Power	11
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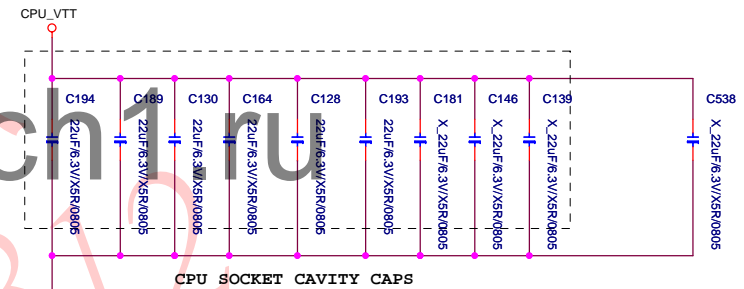
+CPU_VCCP-Decoupling



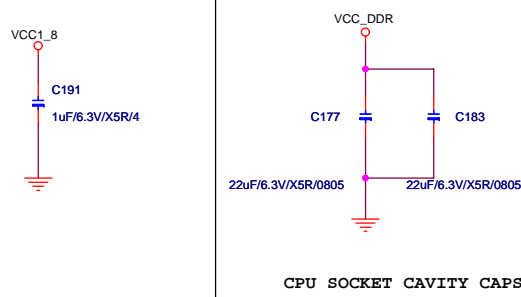
+CPU_GFX Decoupling



+CPU_VTT Decoupling



+1.5V_DDR3-Decoupling

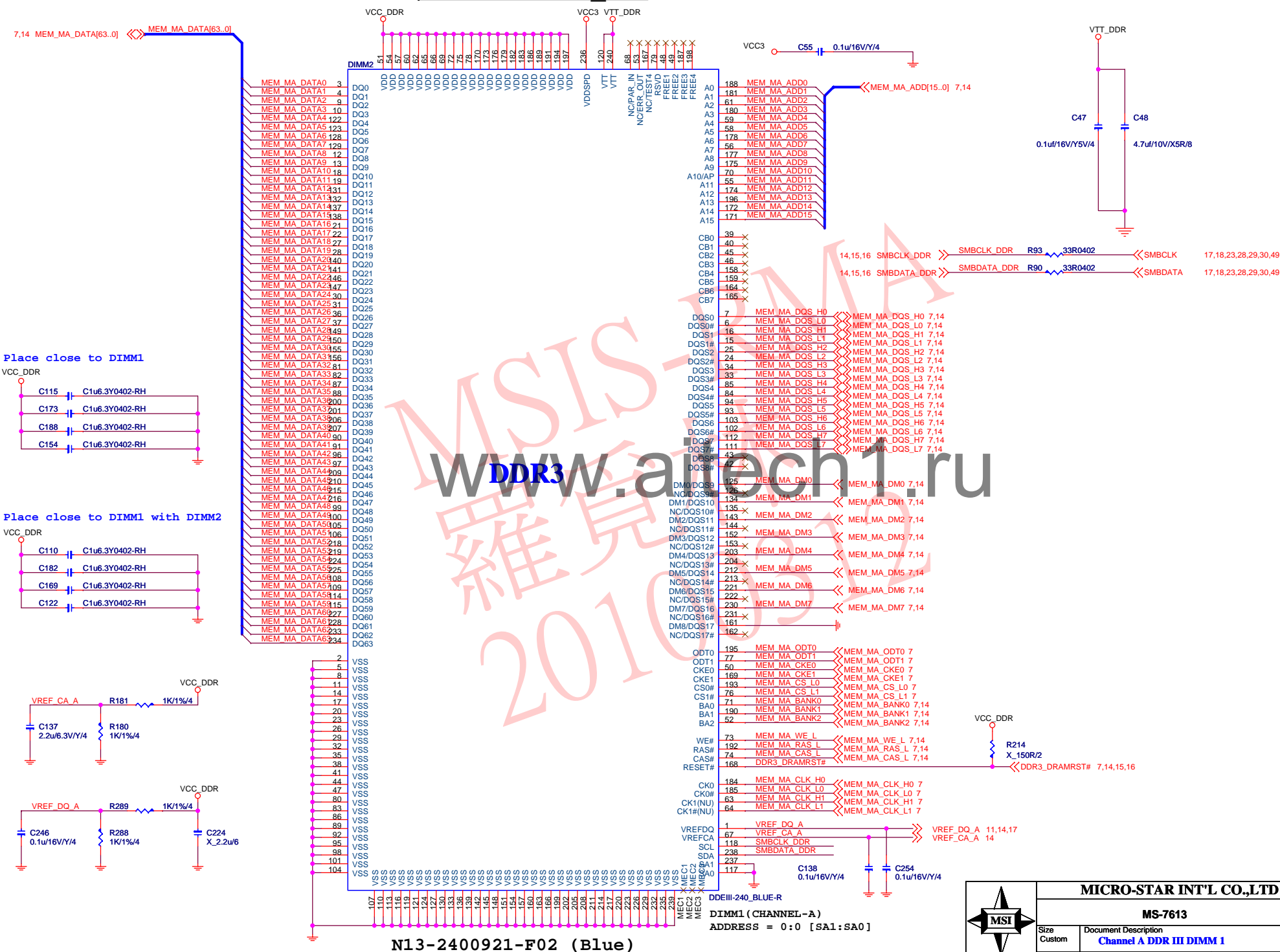


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DDRIII DIMM A1



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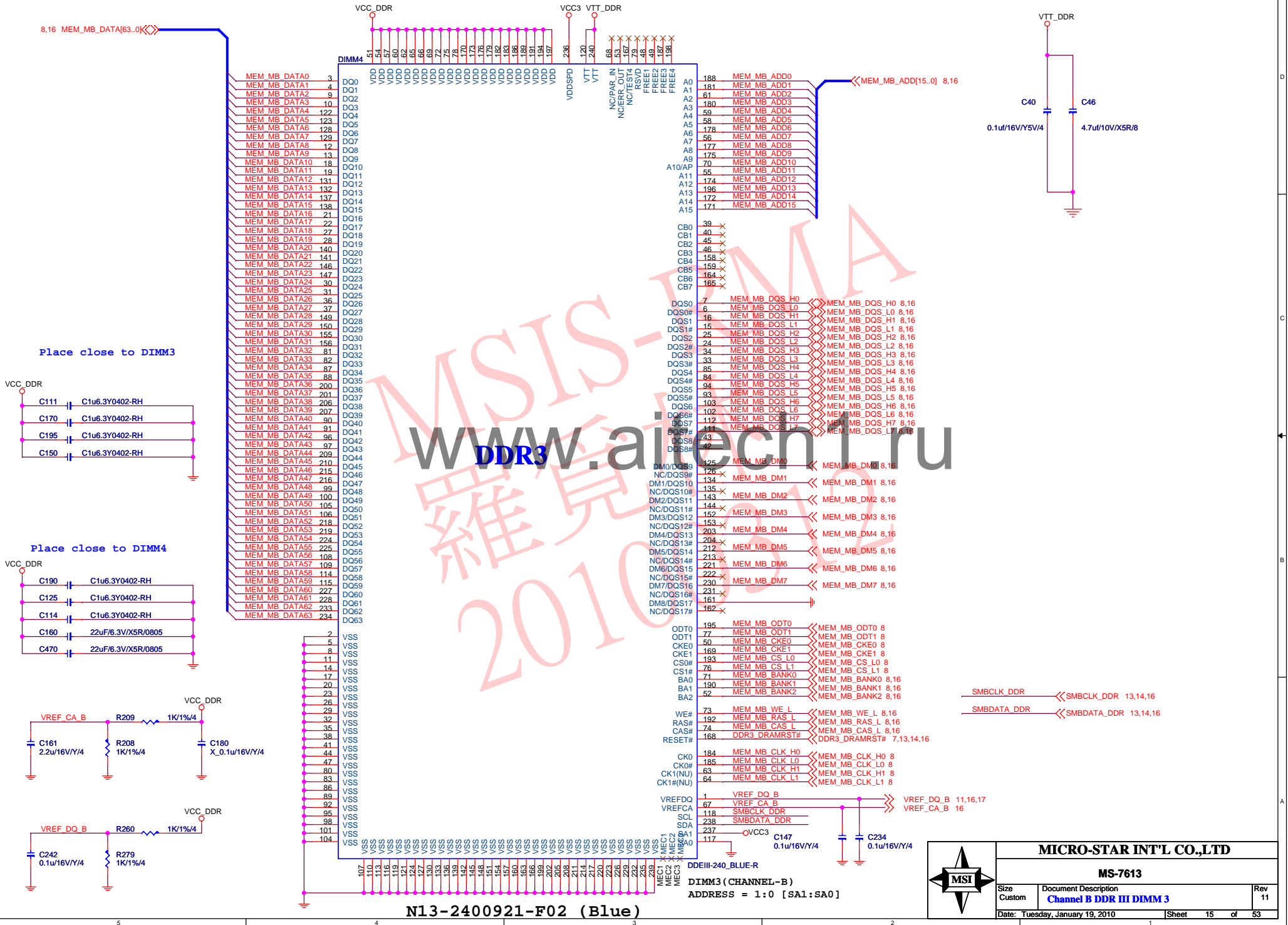
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Size Custom	Document Description Channel A DDR III DIMM 2	Rev 11
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DDRIII DIMM_B1

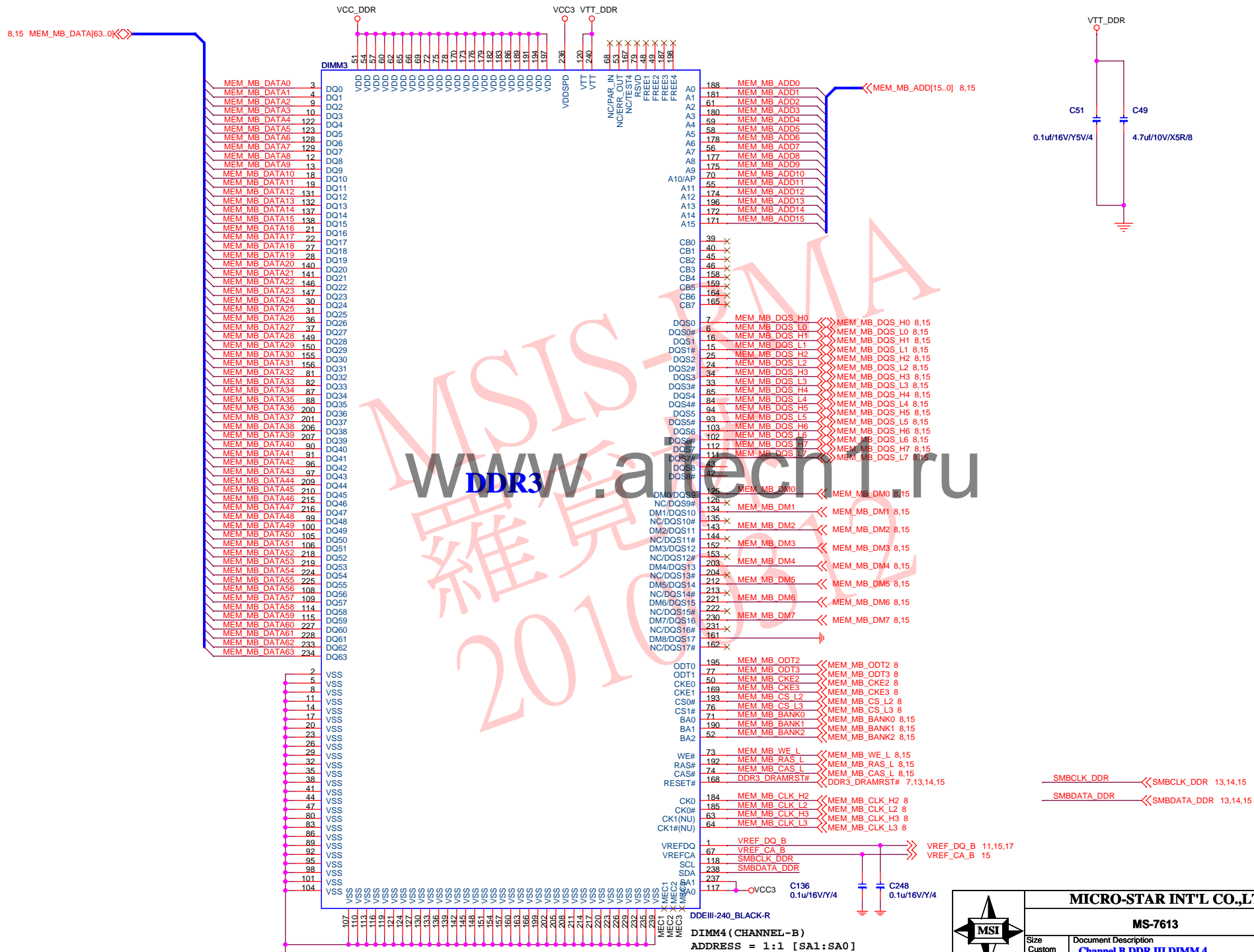


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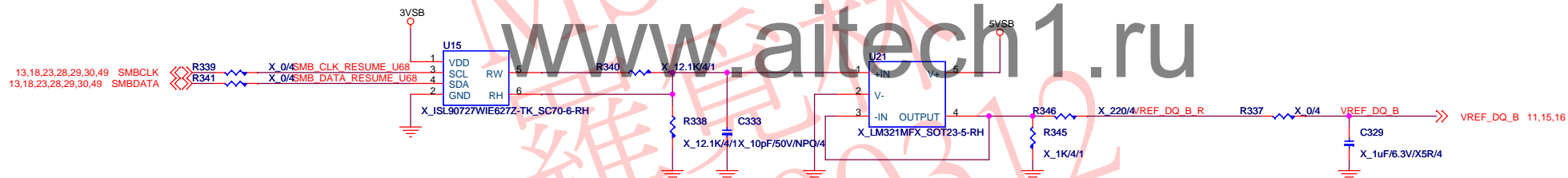
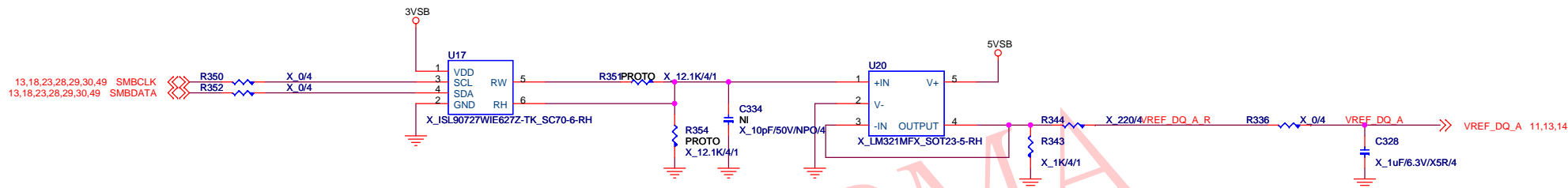


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Size Custom	Document Description Channel B DDR III DIMM 3	Rev 11
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DDRIII DIMM_B2



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Size	Document Description	Rev	
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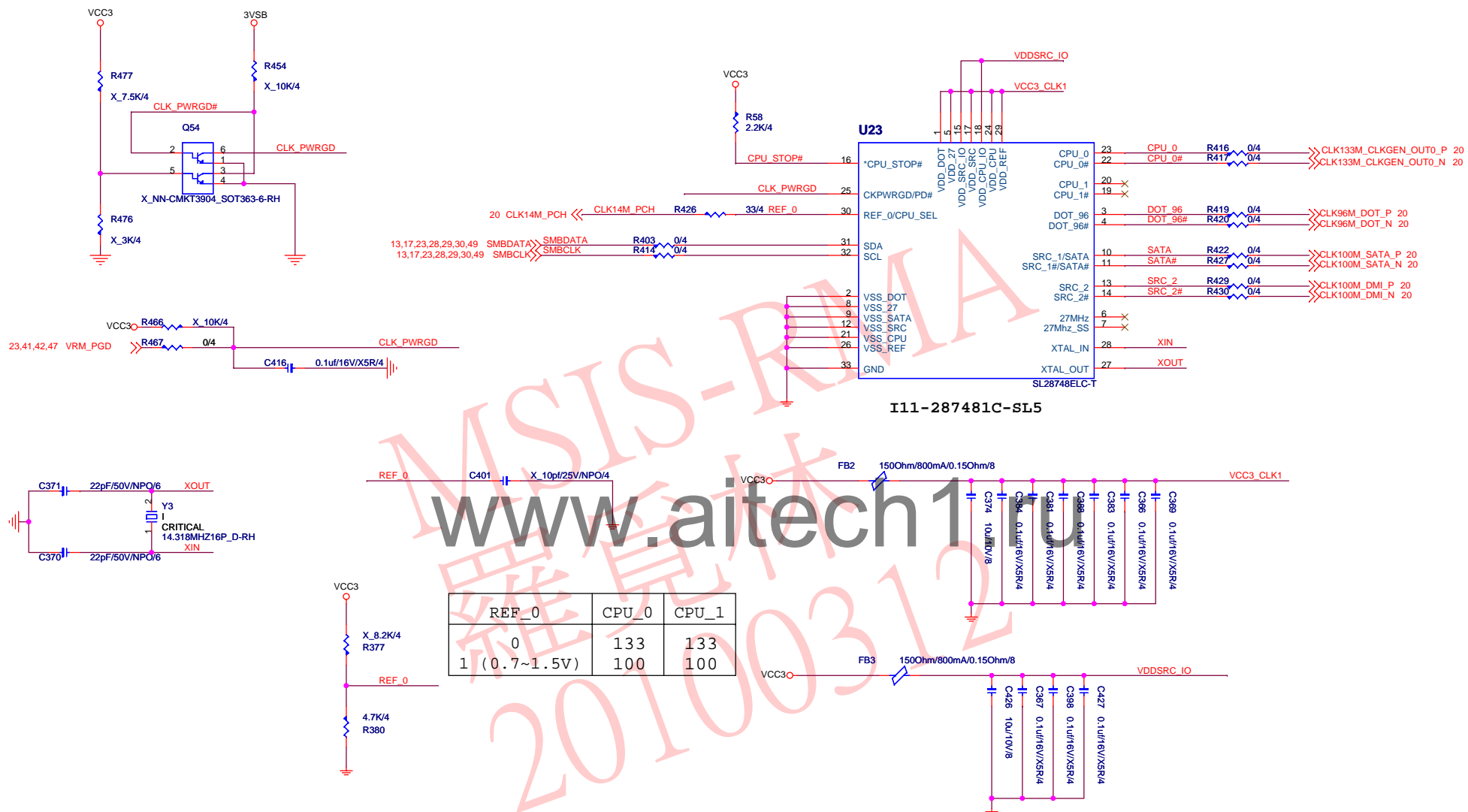


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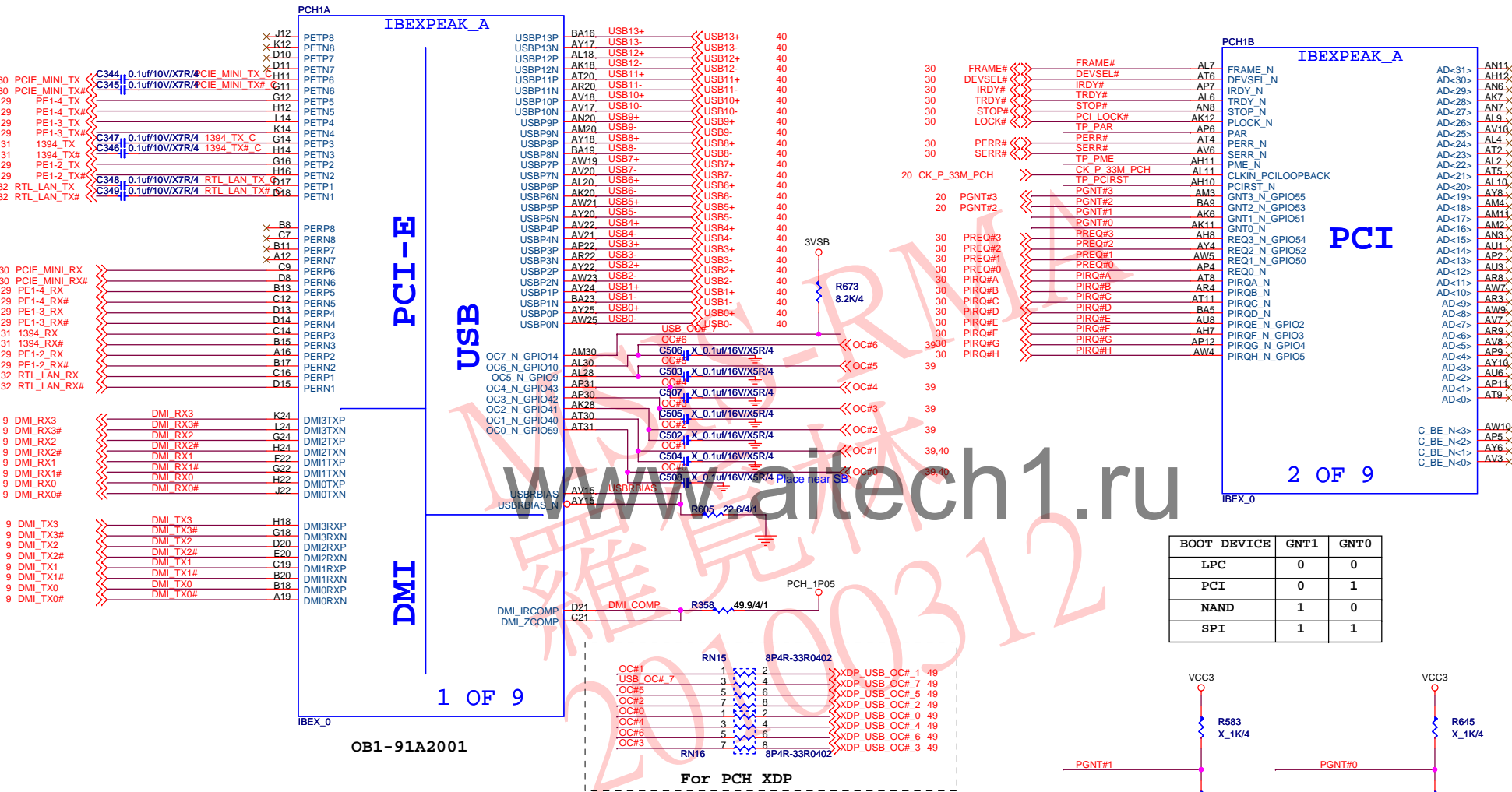
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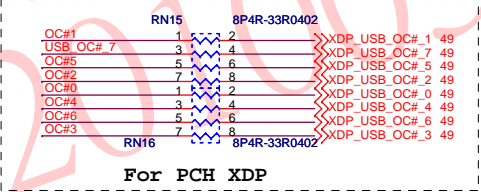
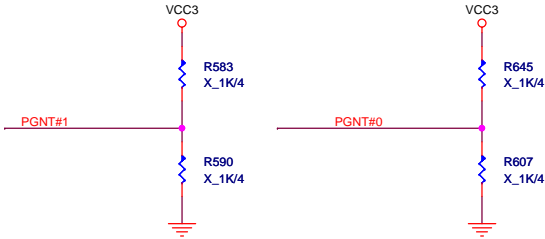
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
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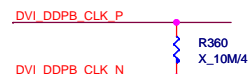
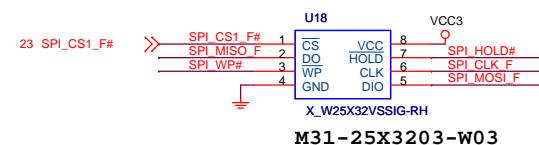
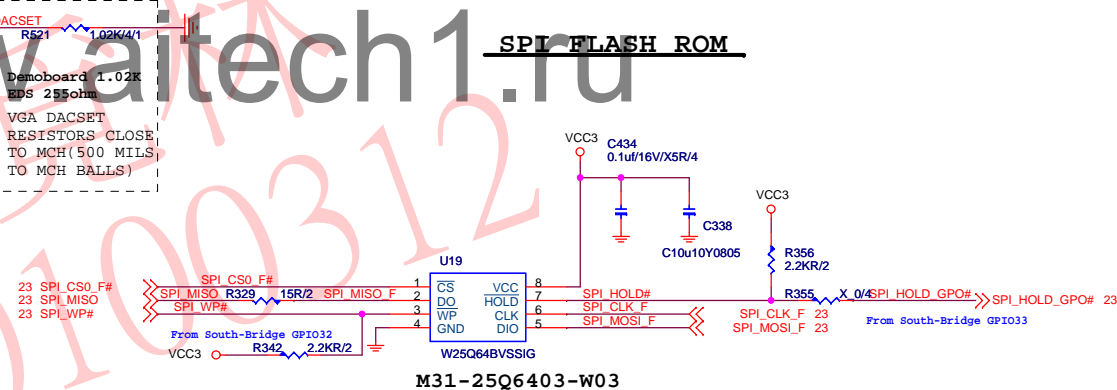


BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1





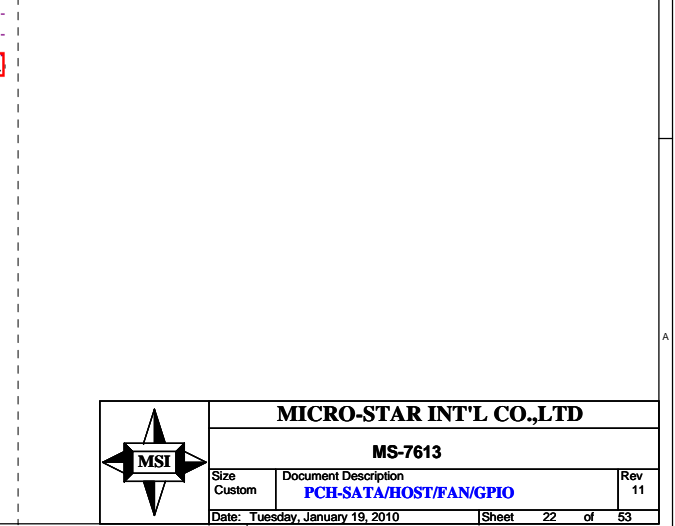
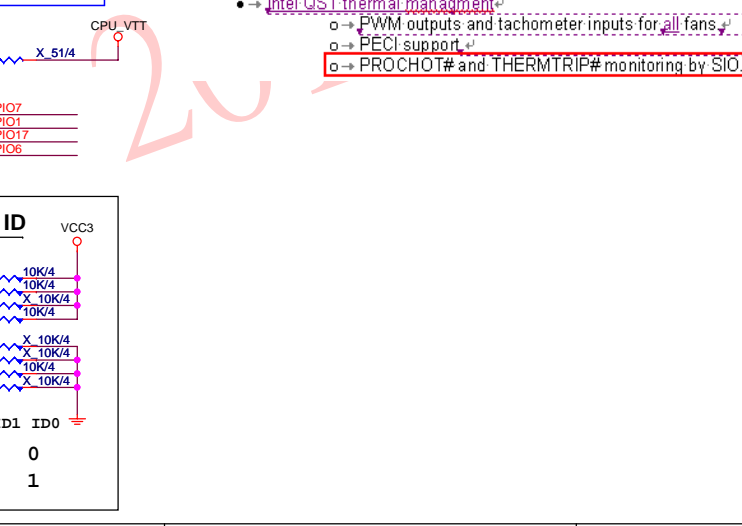
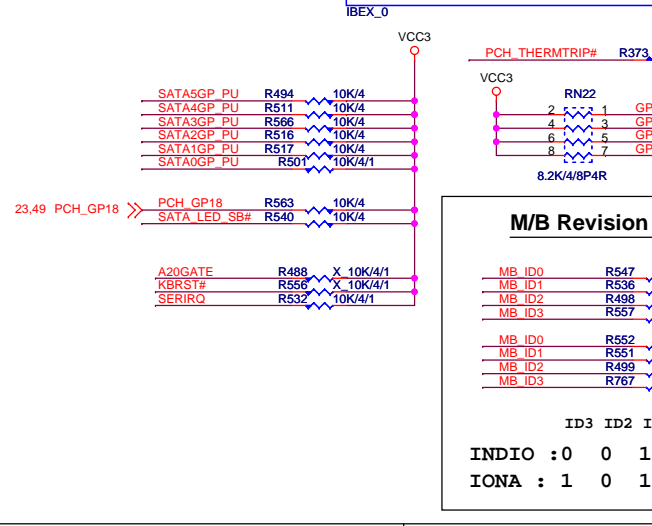
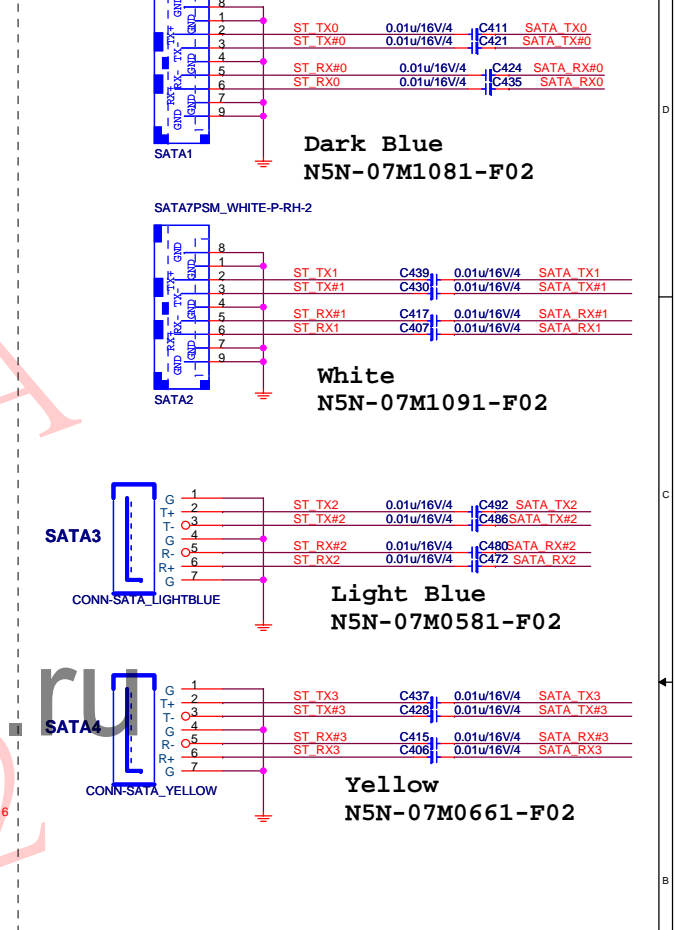
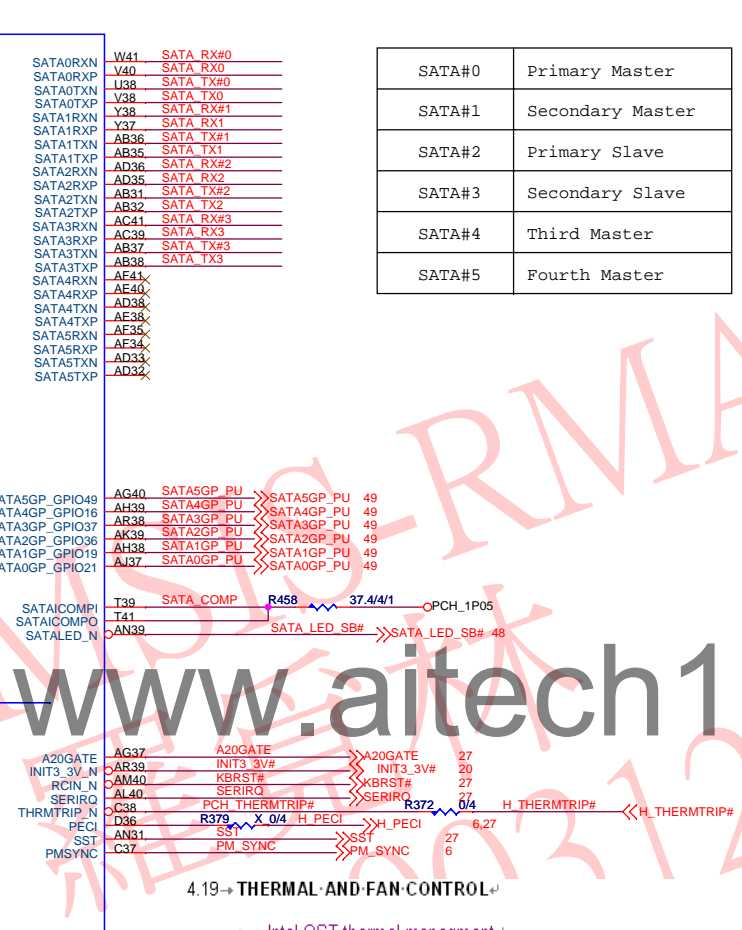
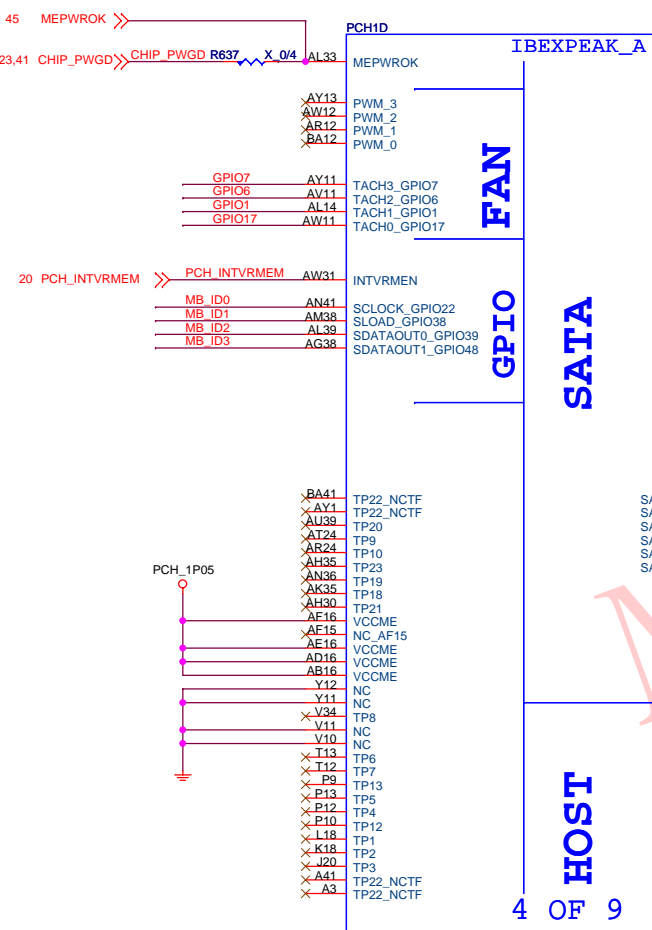
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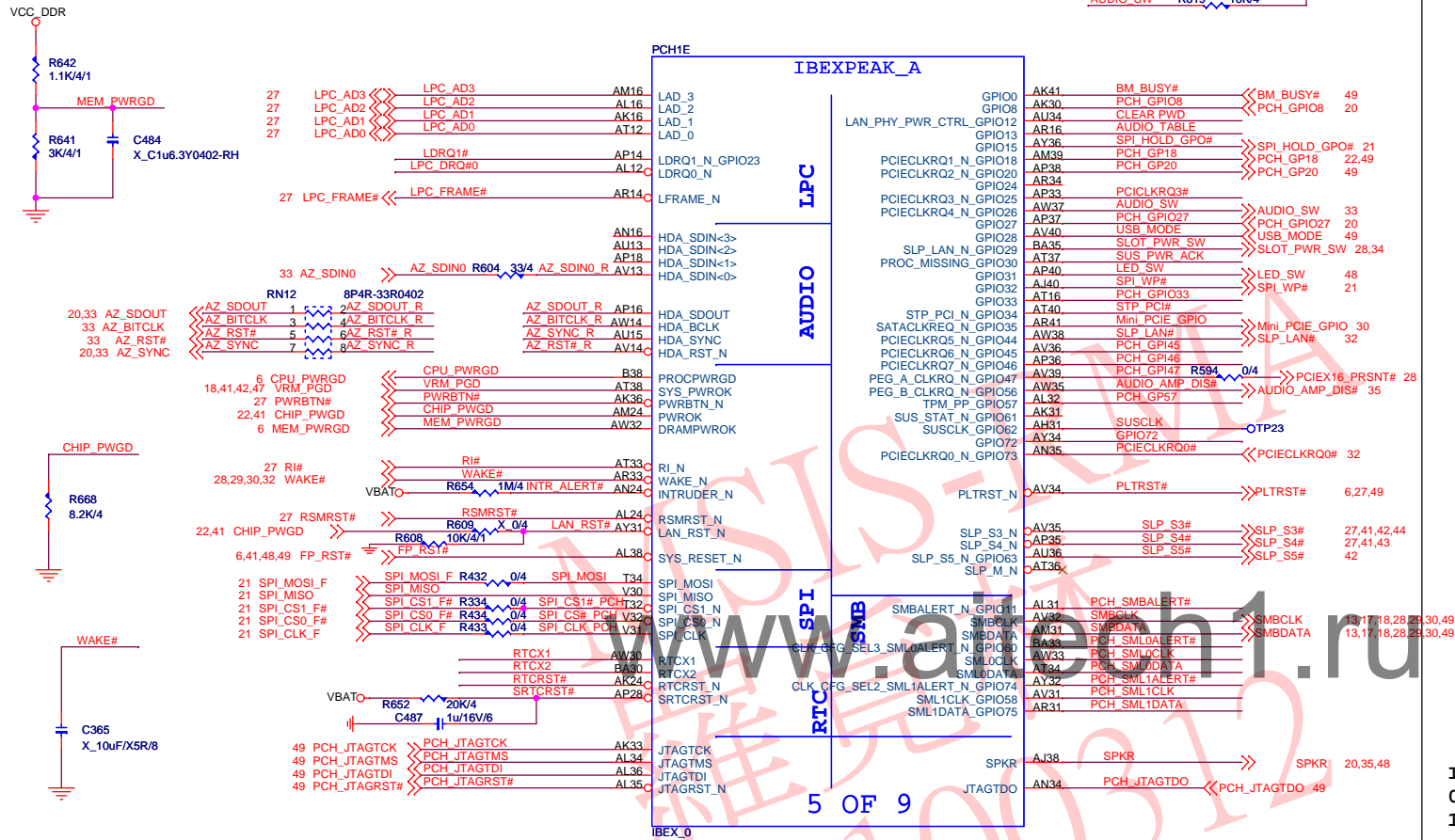


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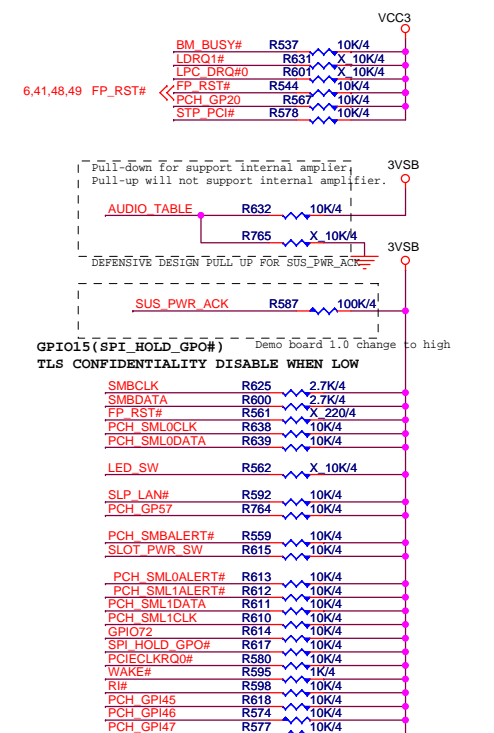
MS-7613

Size Custom	Document Description PCH-DISPLAY/ SPI ROM	Re 1
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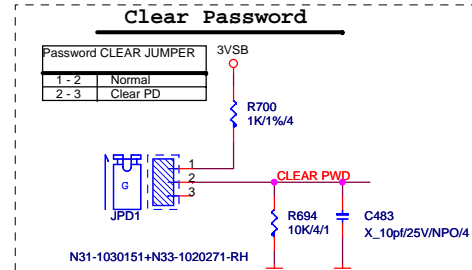
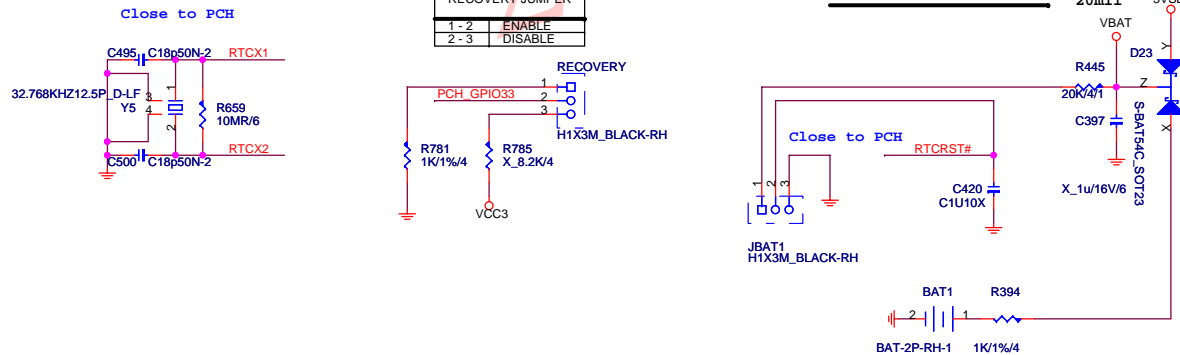


USB MODE R588 10K/4
PCIECLKRQ3# R593 10K/4
AUDIO_SW R619 10K/4



CMOS CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear CMOS

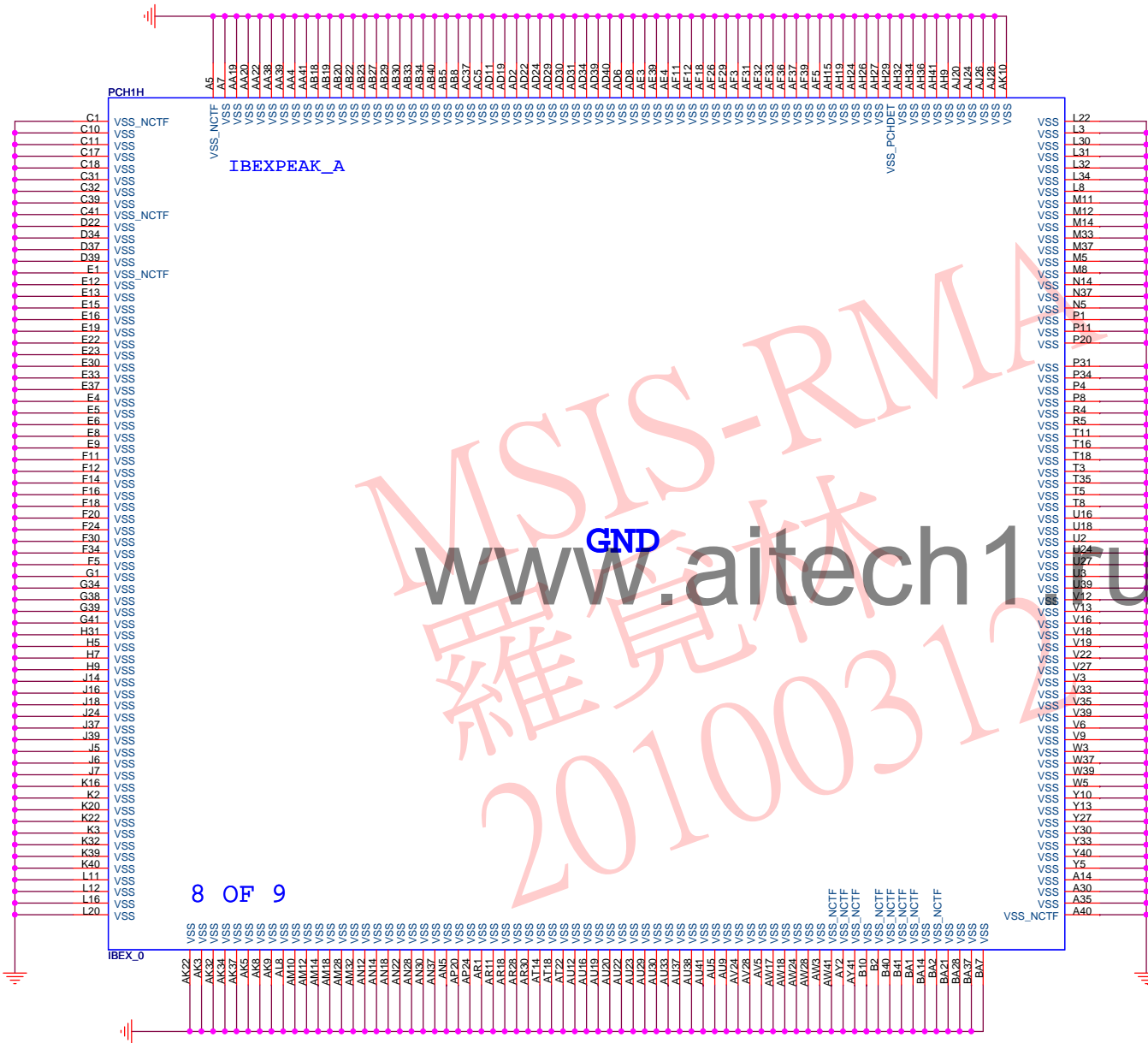
RTC Block



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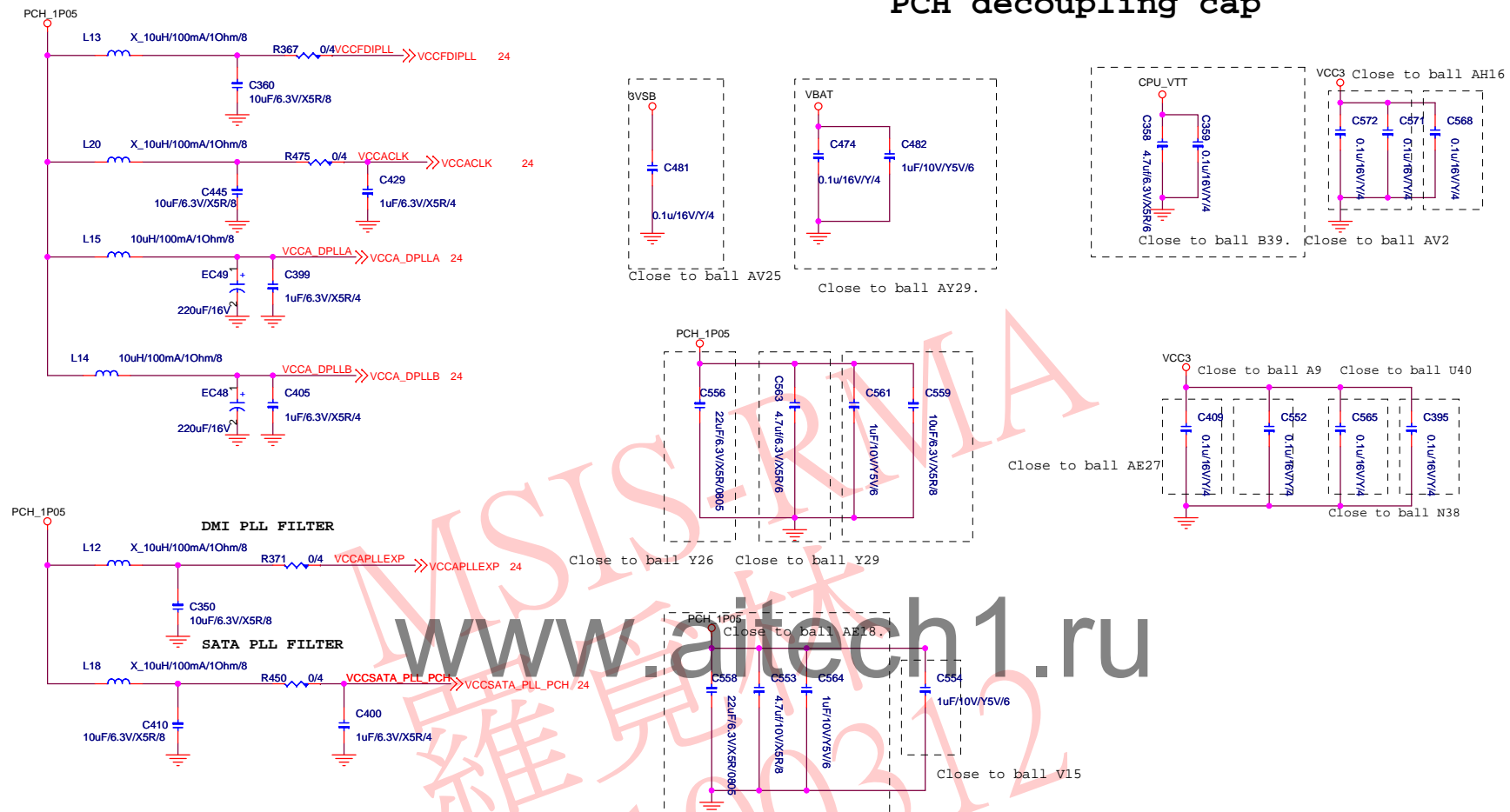
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Size	Document Description	Rev
Custom	PCH-SMB/LPC/AUDIO/RTC	11
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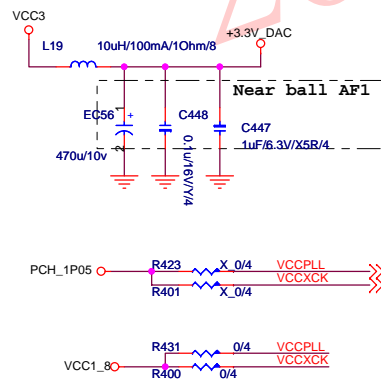
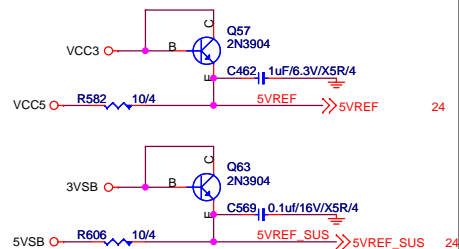
MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size	Document Description	Rev
Custom	PCH-GND	11
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PCH decoupling cap



5VREF & 5VREF_SUS Sequencing Circuit

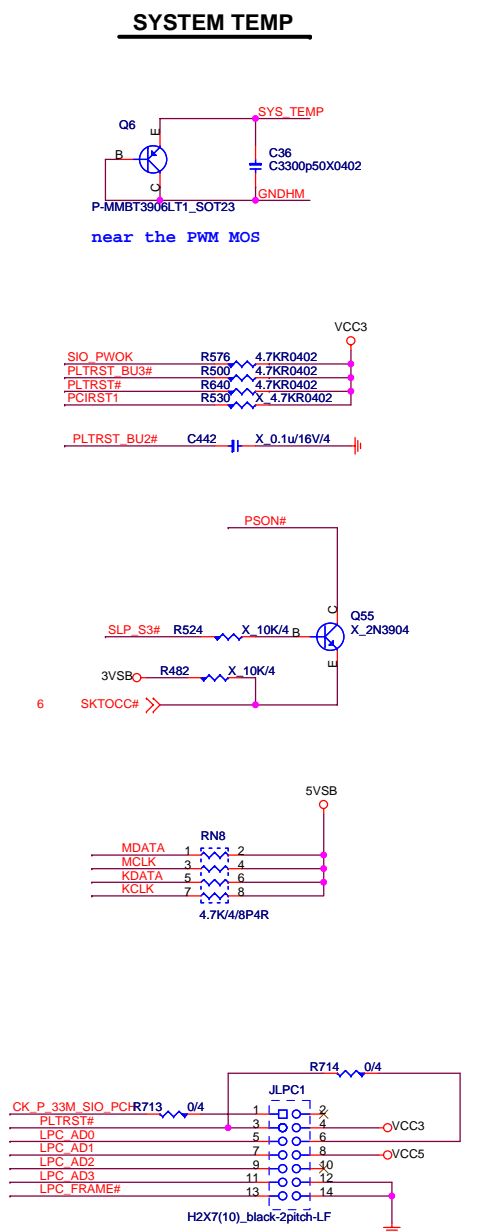
5VREF must be powered up before VCC3 or after VCC3 within 0.7V. Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to 5VREF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



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Size	Document Description	Rev
Custom	PCH-DECOPLING	11
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Pin	Function	Net name	HI	NC
13	FWH_TRAP	IO_CHAS_FAN	Fan control method will be PWM Mode	Fan control method will be DAC Mode

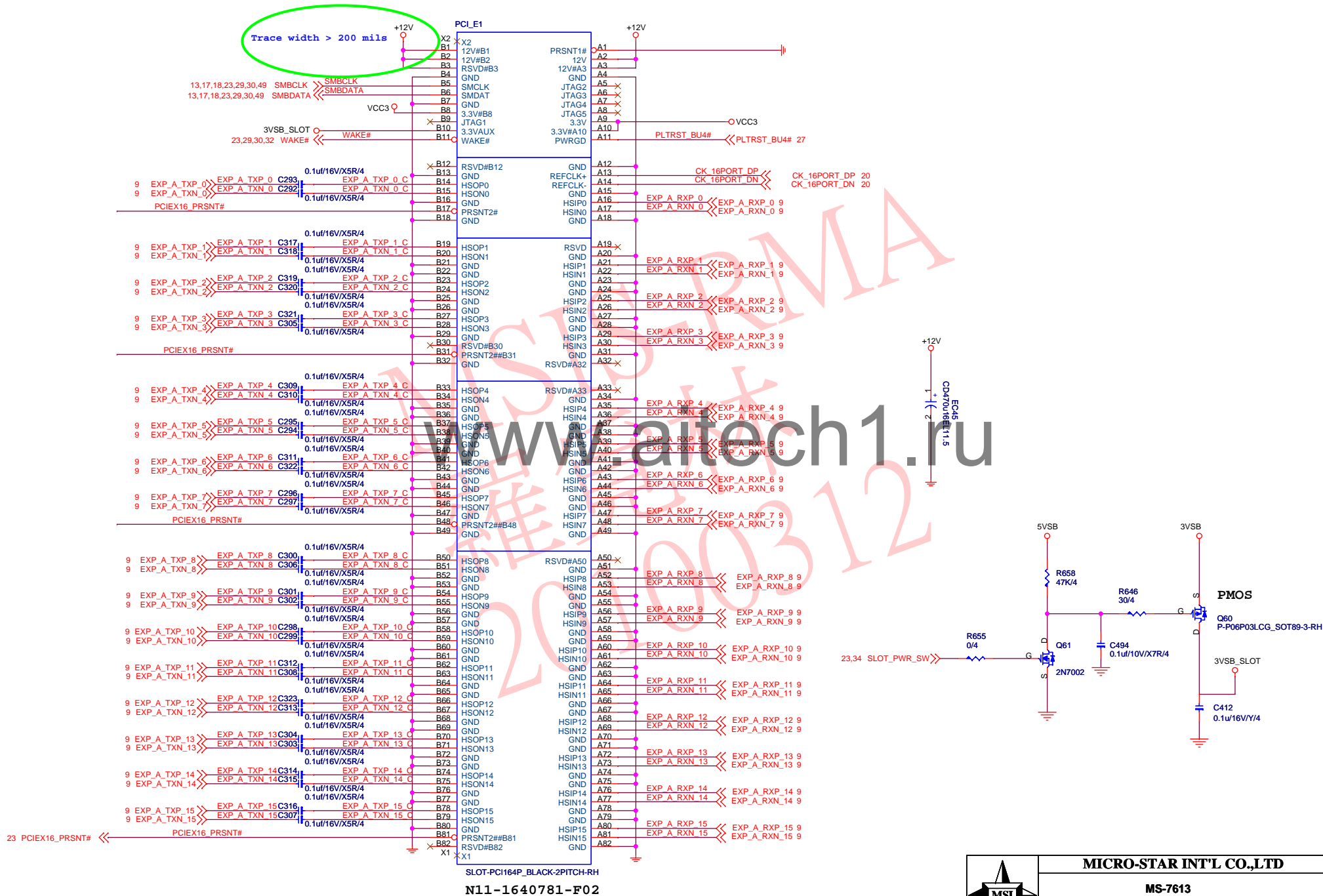


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MS-7613

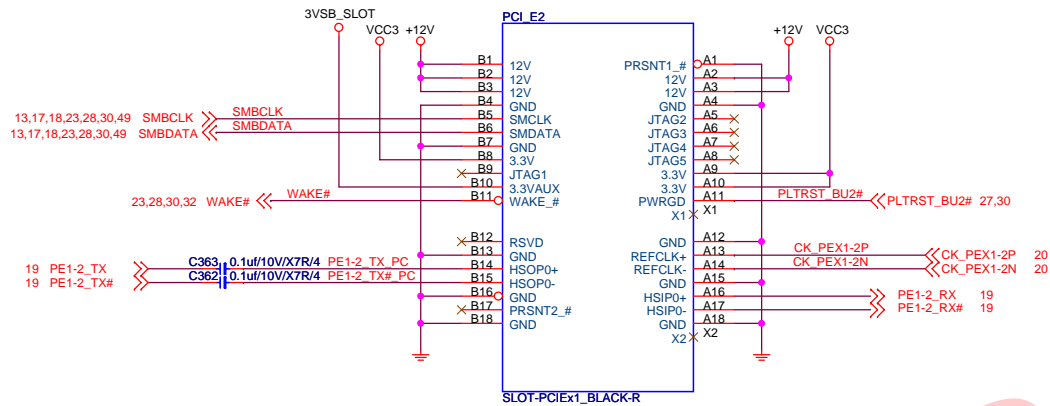
Size Custom	Document Description IO-Fintek F71858D	Rev 11
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PCI Express X16 Slot



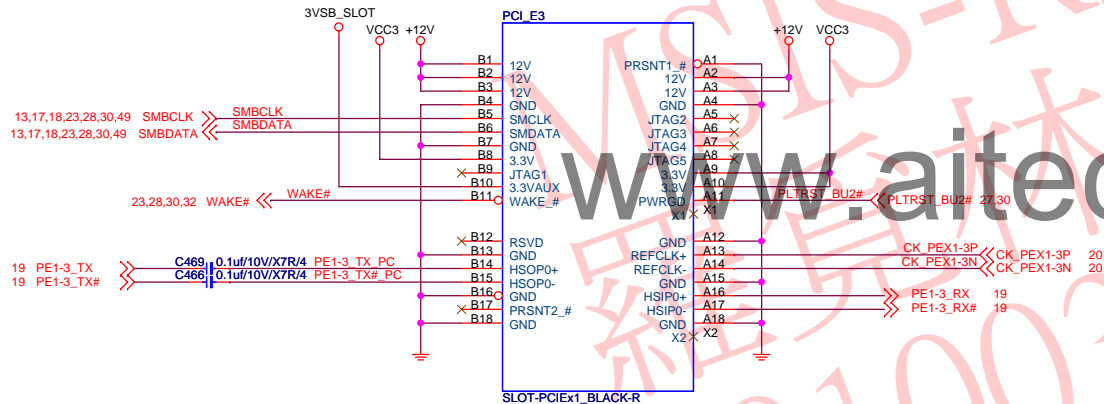
MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size	Document Description	Rev
Custom	PCIE X16 SLOT	11
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PCI EXPRESS x1-PORT1



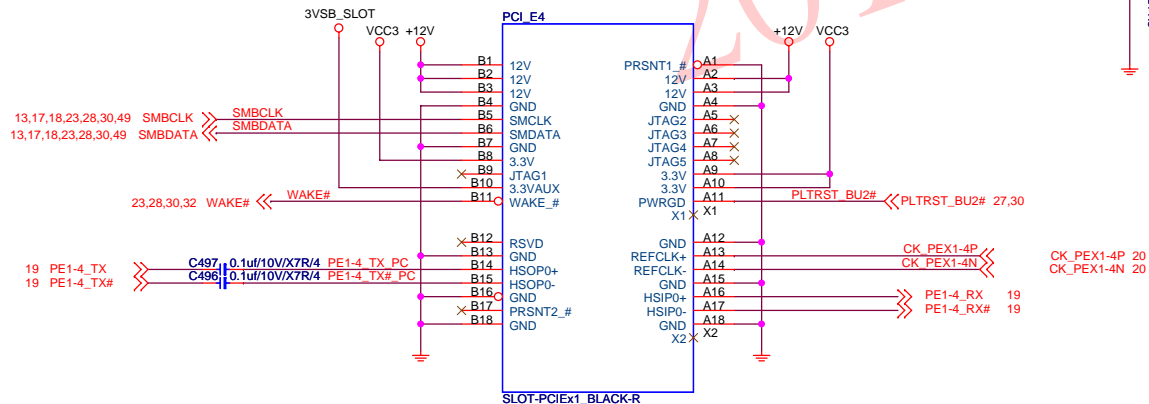
N11-0360281-K06

PCI EXPRESS x1-PORT2



N11-0360281-K06

PCI EXPRESS x1-PORT3



N11-0360281-K06

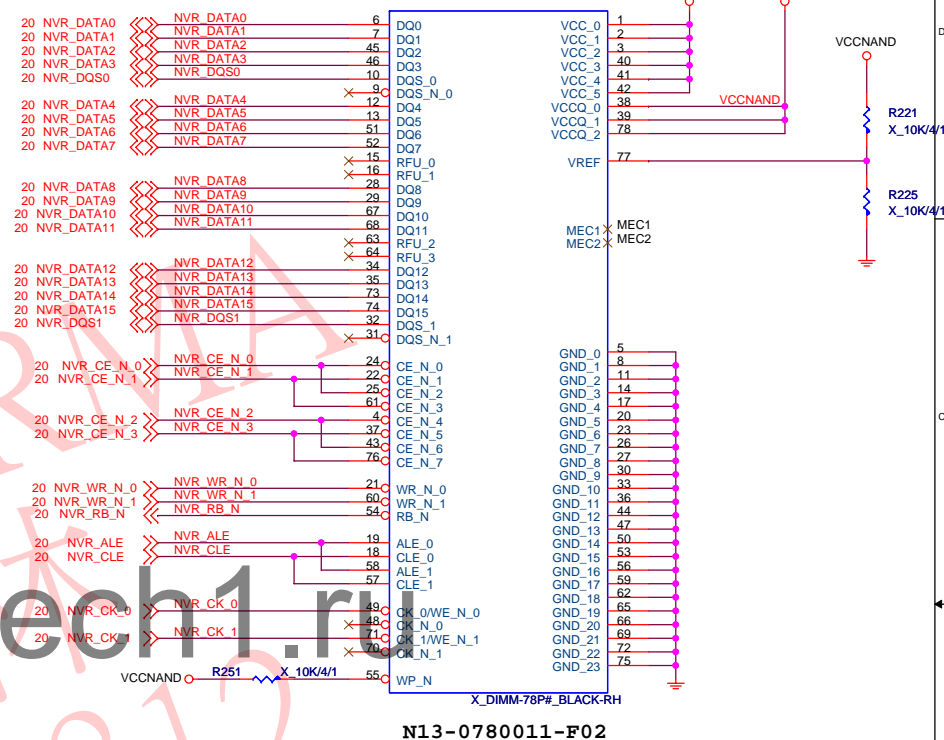
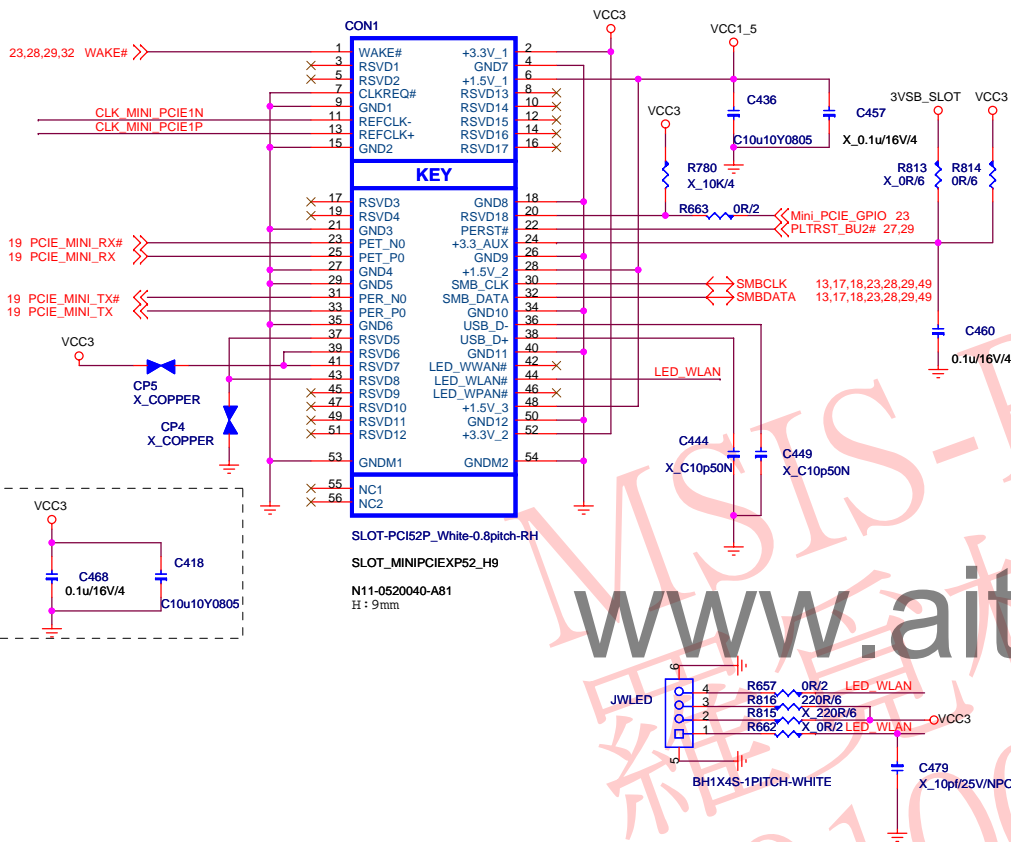


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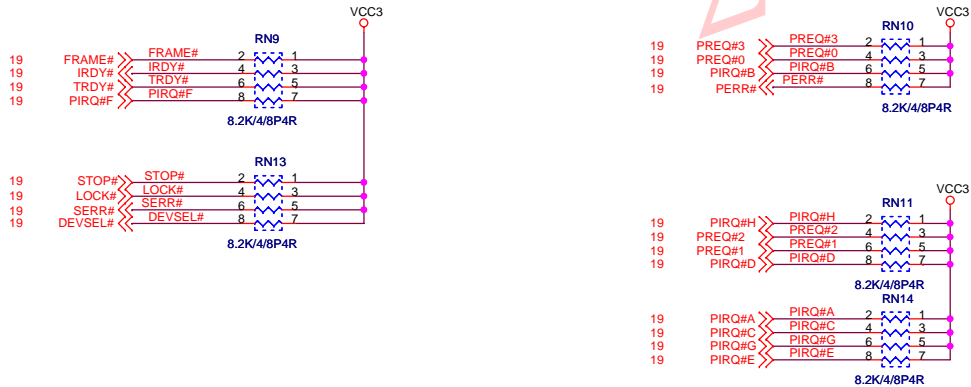
MS-7613

Size	Document Description	Rev
Custom	PCIE X1 SLOT	11
Date:	Tuesday, January 19, 2010	Sheet 29 of 53

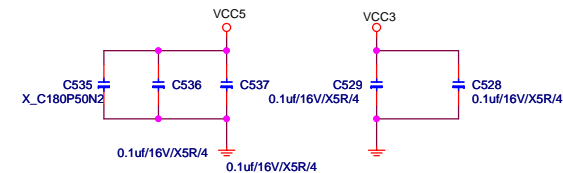
20 CLK_MINI_PCIE1N
20 CLK_MINI_PCIE1P



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

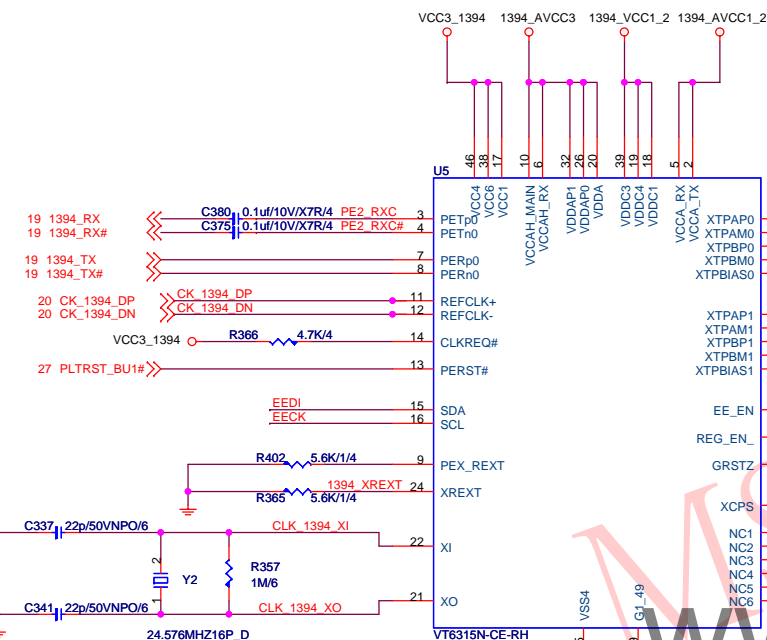


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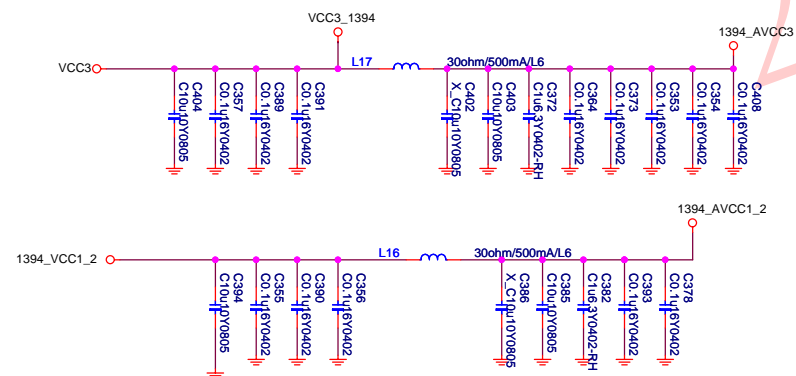
Size	Document Description	Rev
Custom	Mini PCIe Slot & ONFI Slot	11
Date: Tuesday, January 19, 2010	Sheet 30 of 53	

1394 CONTROLLER

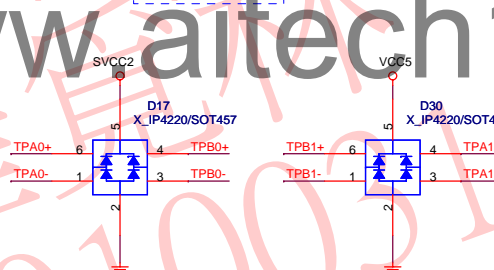
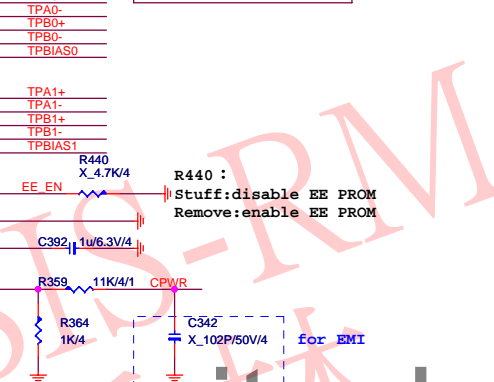
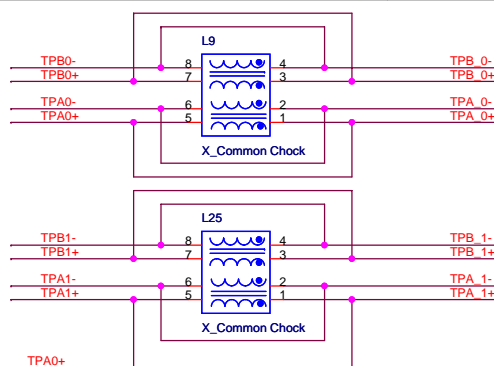


B07-6315N1C-V01

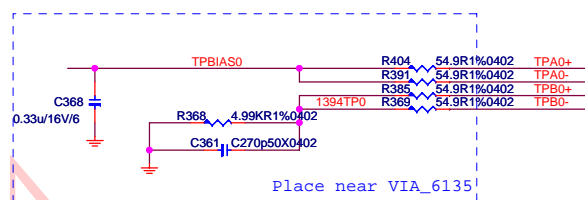
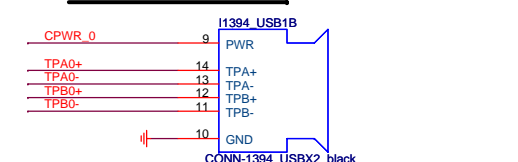
close to chip of all Cap.



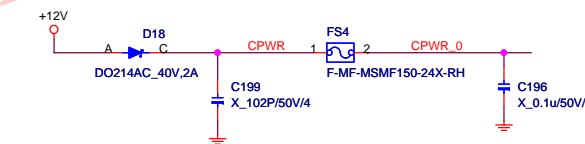
close to chip of all Cap.



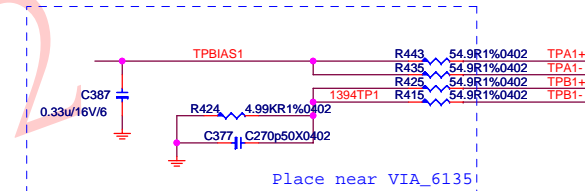
Rear 1394 port



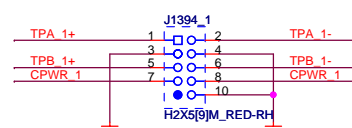
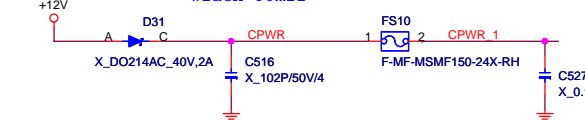
width 60mil



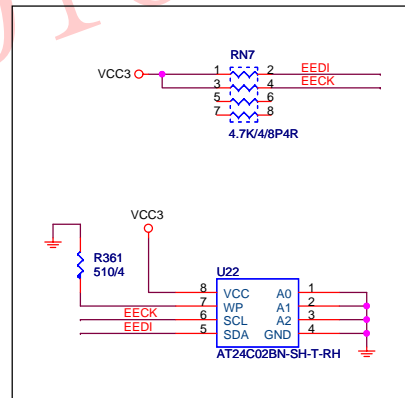
Front 1394 pin header



width 60mil



For Intel 1394 pinheader

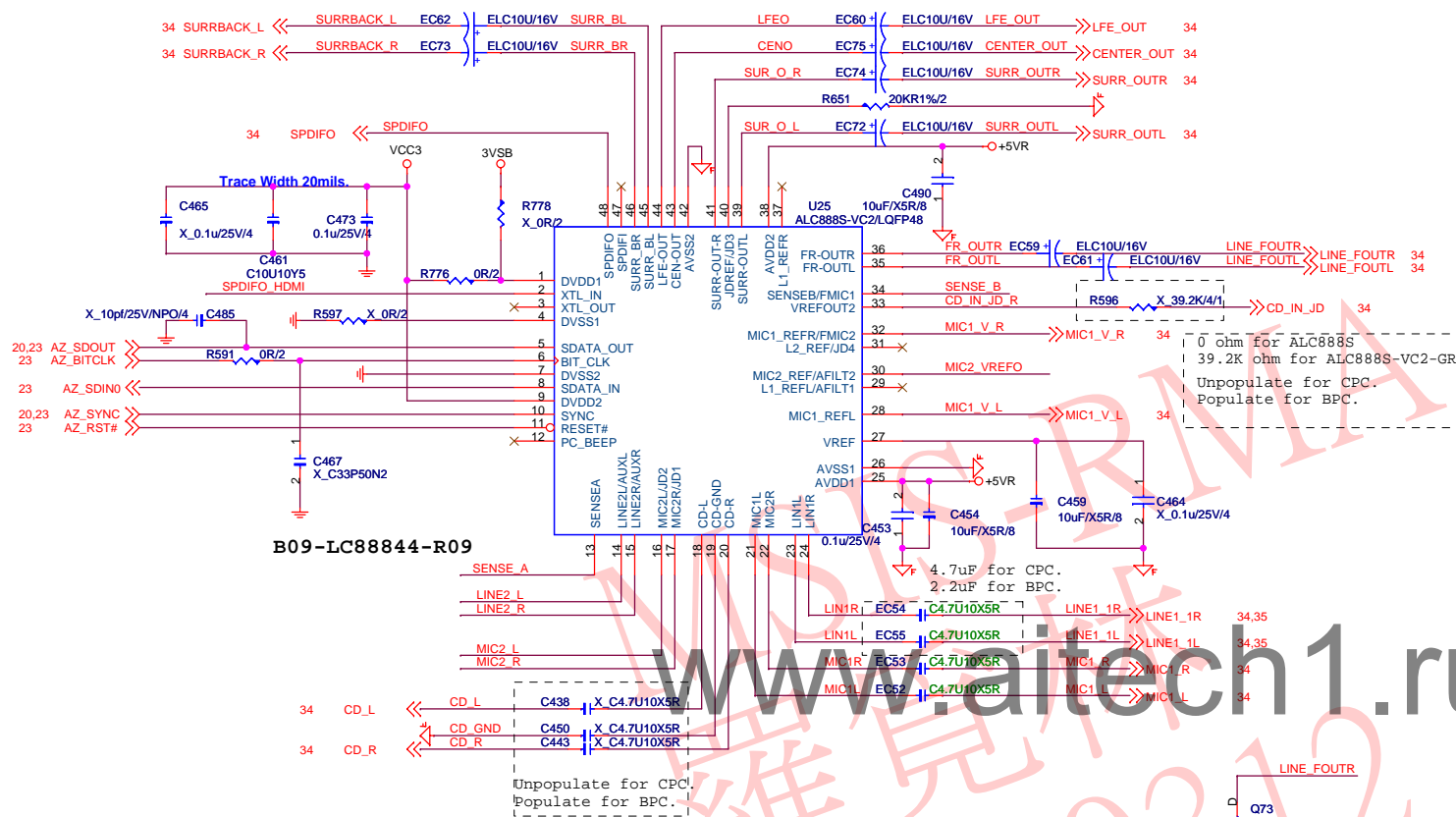


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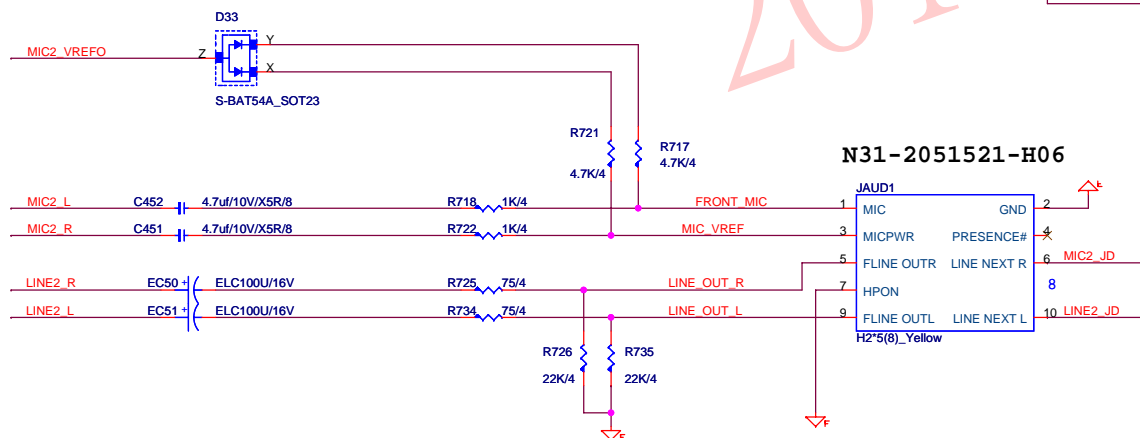
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Size	Document Description	Rev
Custom	1394 Controller - VT6315N-CE	11
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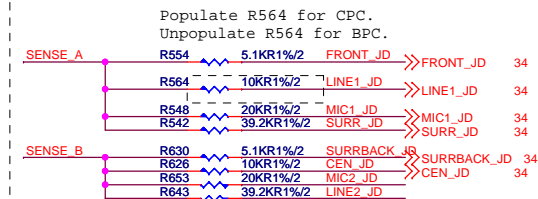
ALC888S CODEC



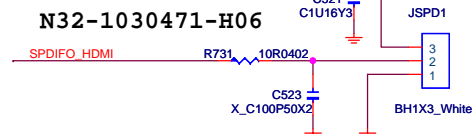
Azalia Front Audio Connector



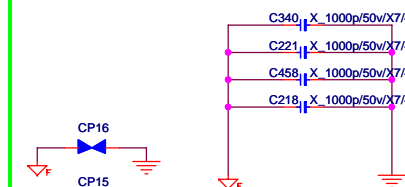
ALC888S JACK DETECT



SPDIF_OUT



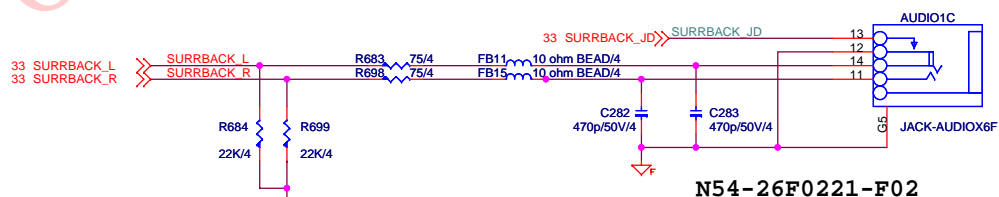
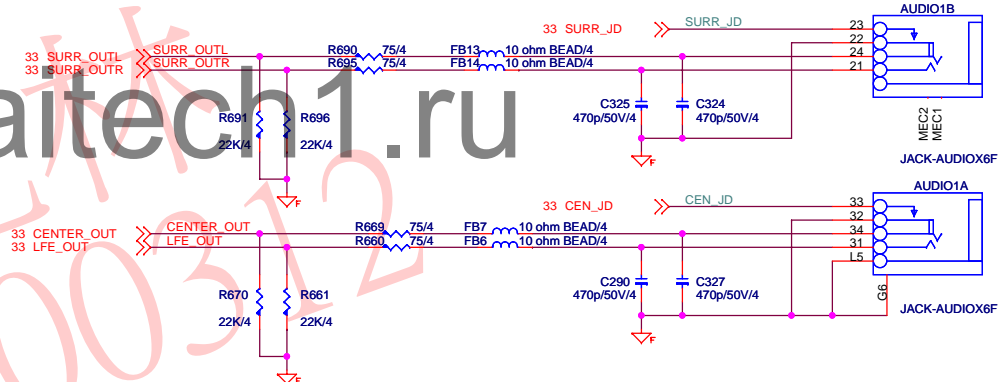
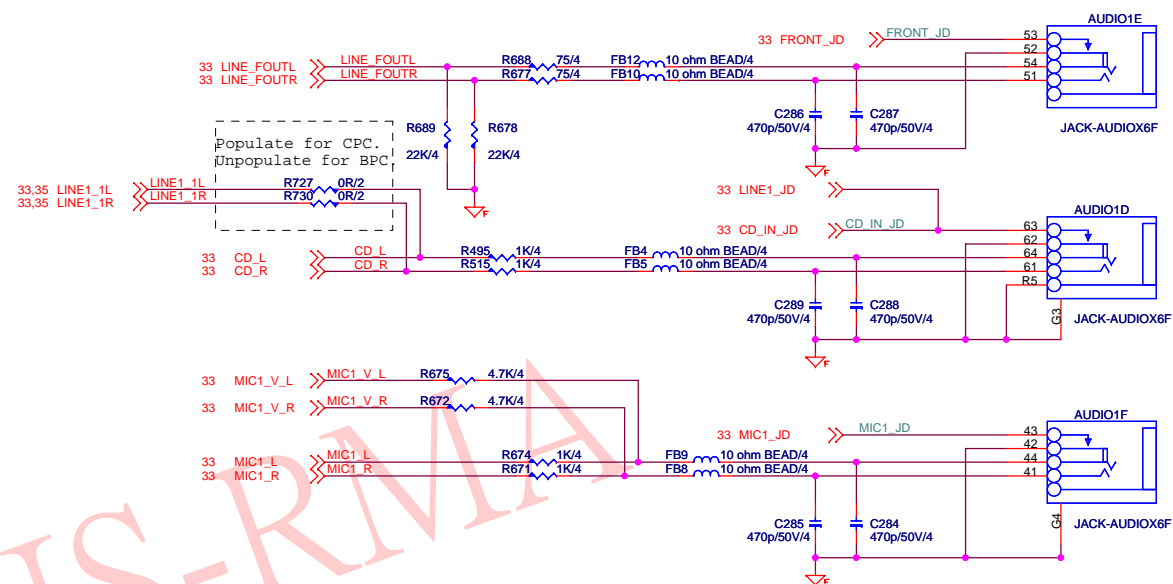
For EMI

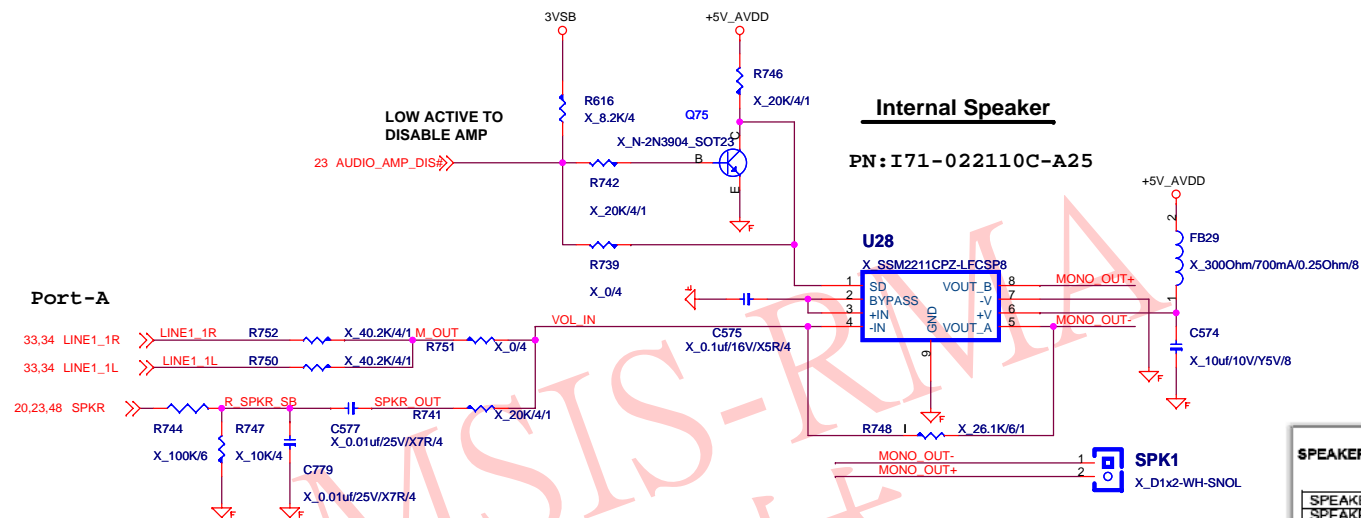


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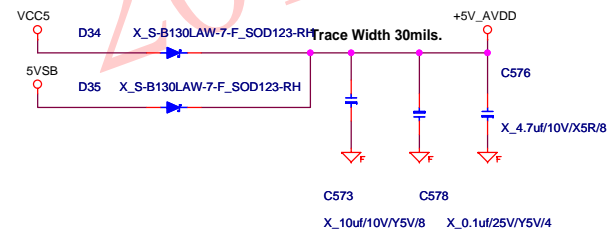
Size	Document Description	Rev
Custom	Audio Codec ALC888S-VC2	11
Date: Tuesday, January 19, 2010	Sheet 33 of 53	





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AUDIO AMPLIFIER POWER REGULATORS

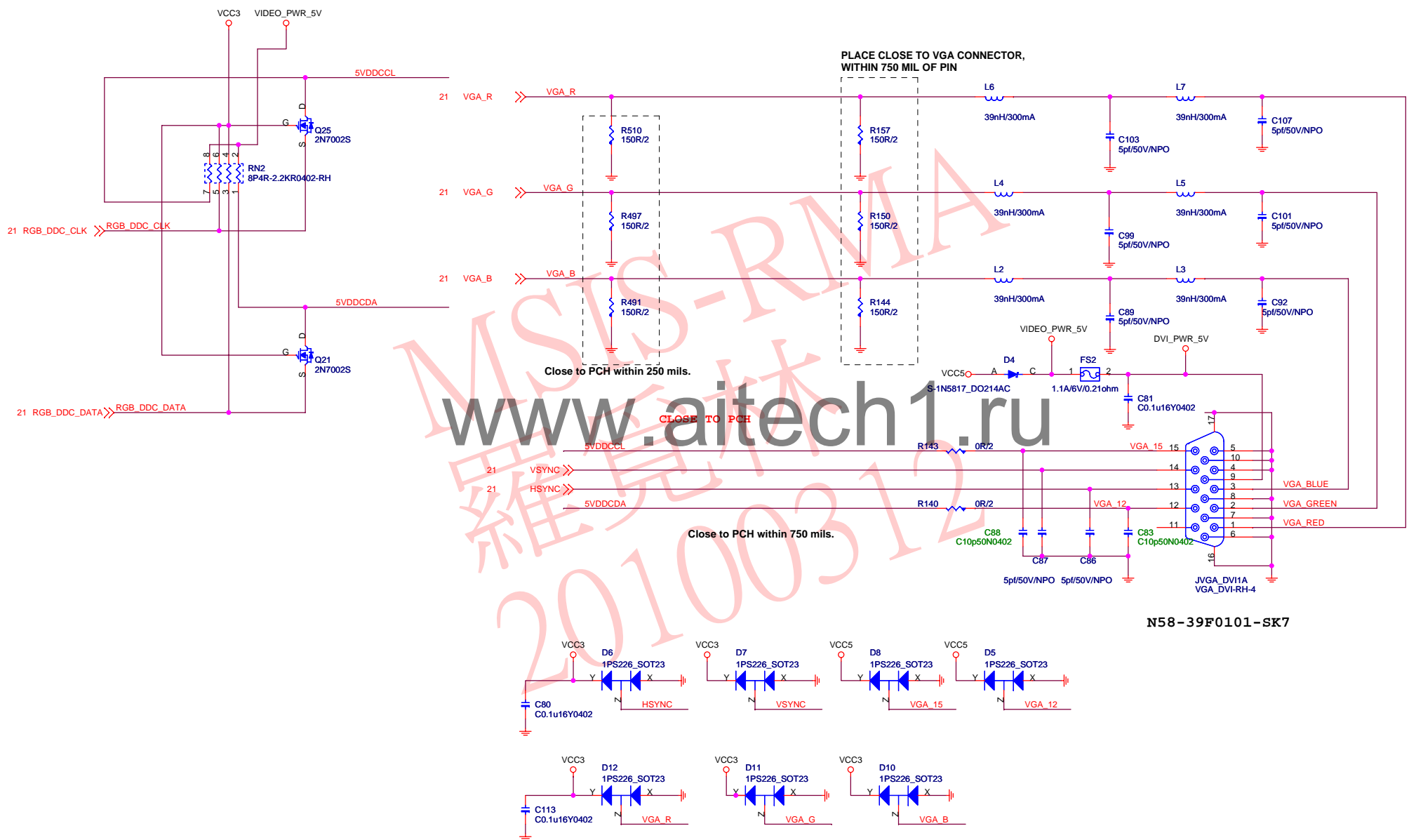


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Size Custom	Document Description AUDIO AMPLIFIER	Rev 11
Date: Tuesday, January 19, 2010	Sheet 35 of 53	

Video Connector

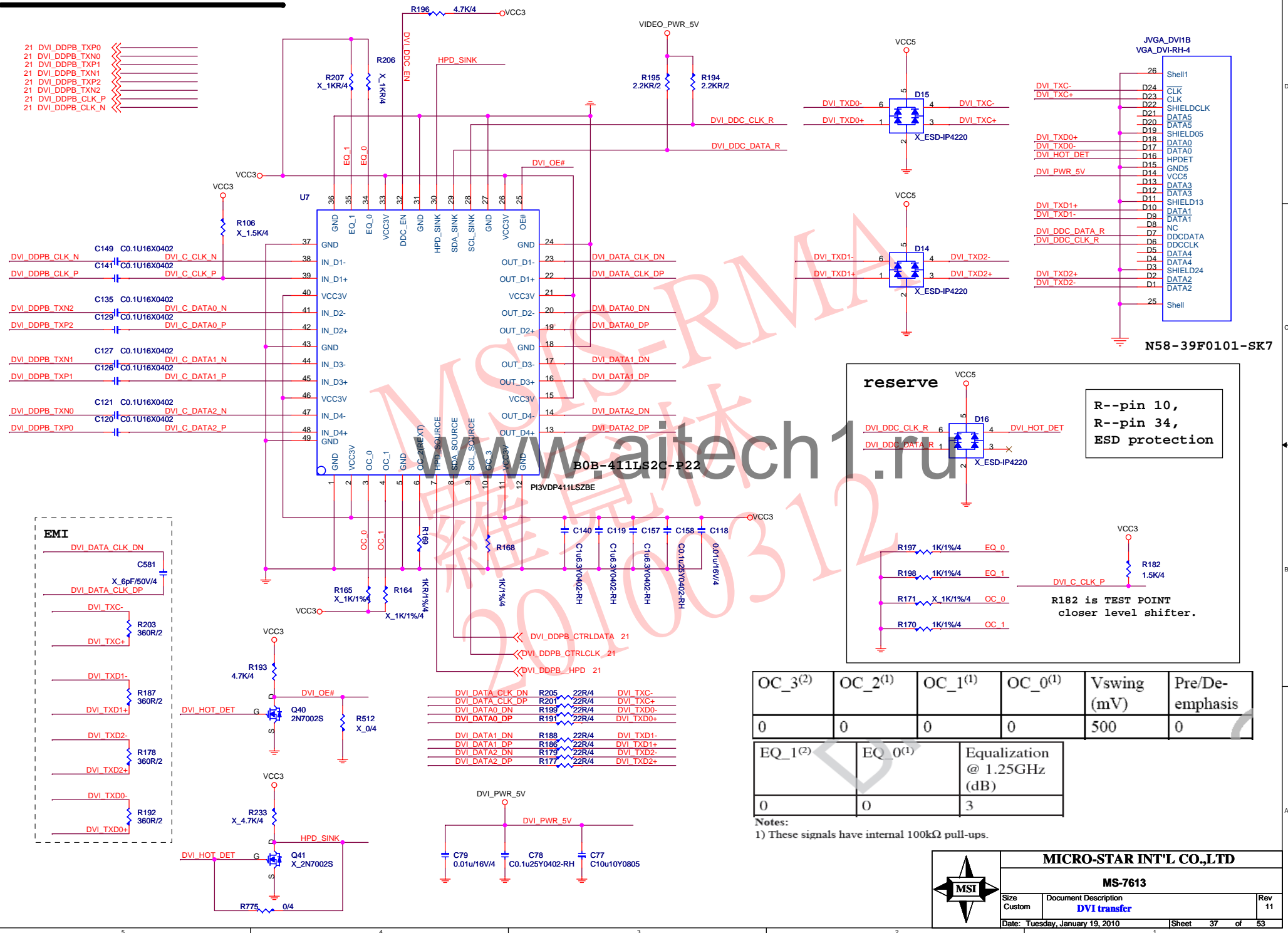


MICRO-STAR INT'L CO.,LTD

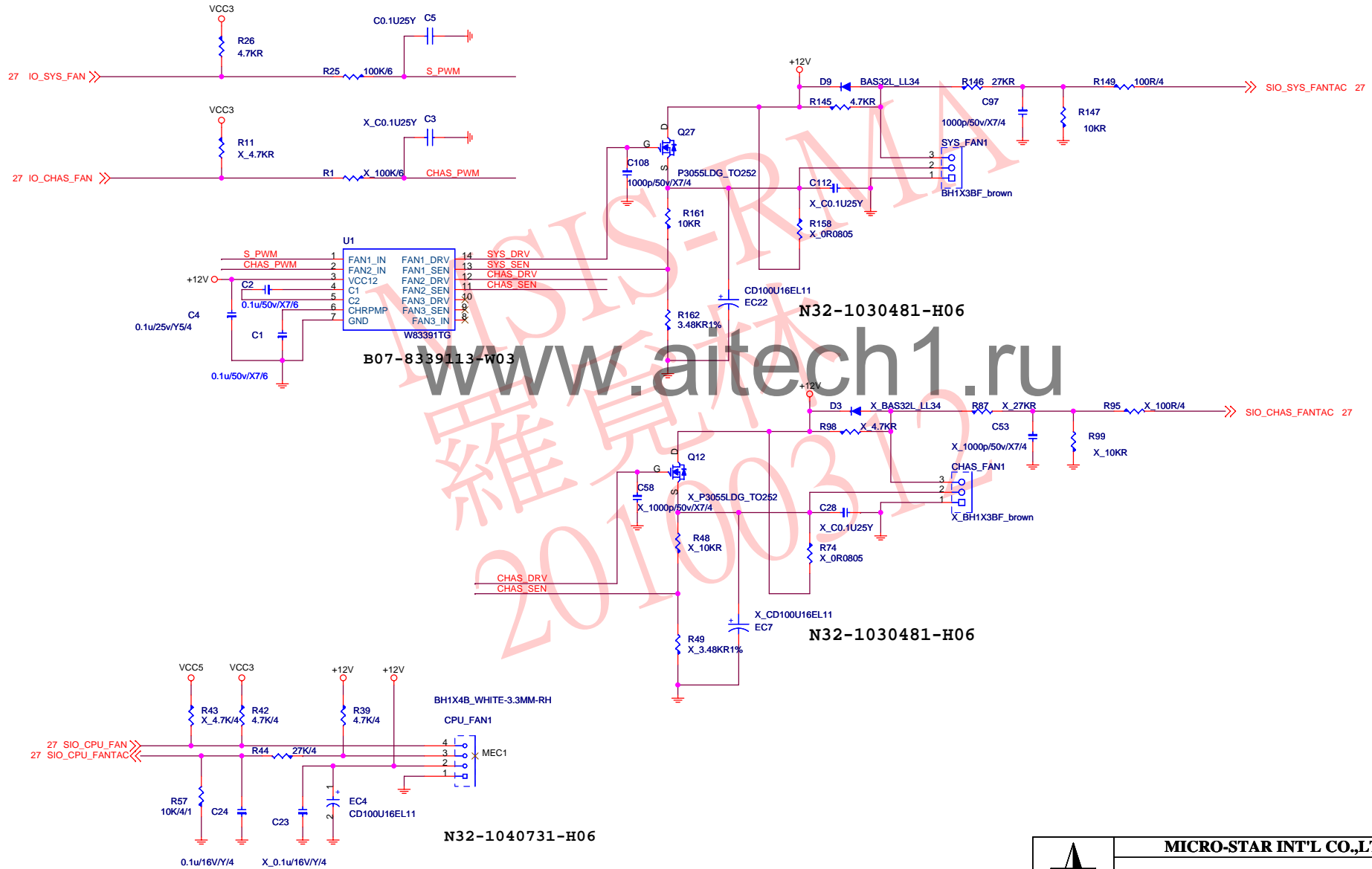
MS-7613

Size	Document Description	Rev
Custom	VGA	11
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DVI level shifter



FAN-COUNTROL CIRCUIT

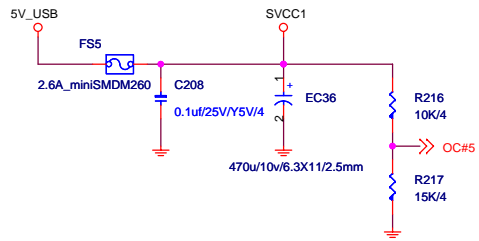


MICRO-STAR INT'L CO.,LTD

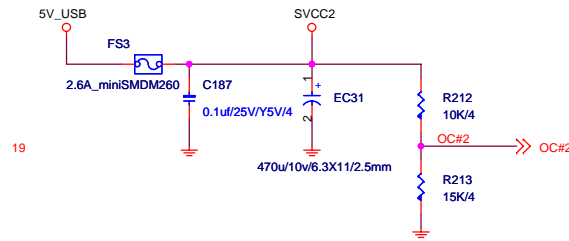
MS-7613

Size	Document Description	Rev
Custom	FAN Control	11
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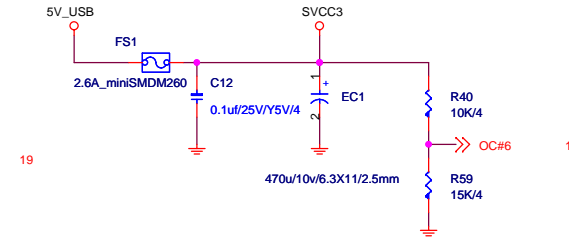
POWER CIRCUIT FOR USB PORT 10, 11



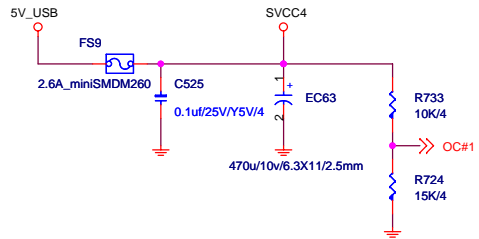
POWER CIRCUIT FOR USB PORT 4, 5



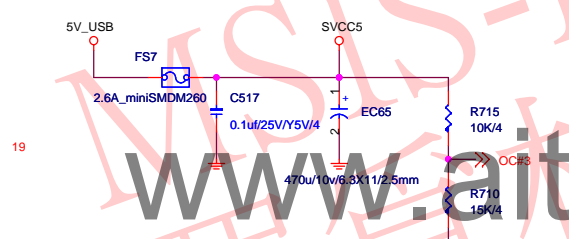
POWER CIRCUIT FOR USB PORT 12, 13



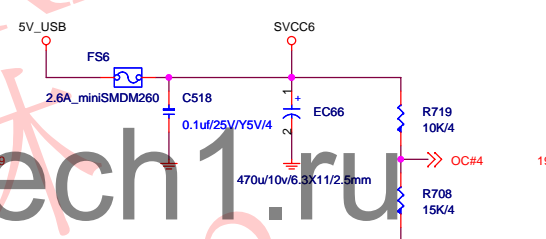
POWER CIRCUIT FOR USB PORT 2, 3



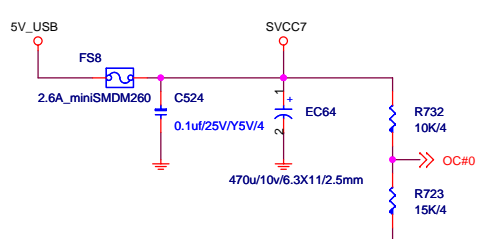
POWER CIRCUIT FOR USB PORT 6, 7



POWER CIRCUIT FOR USB PORT 8, 9



POWER CIRCUIT FOR USB PORT 0, 1



MICRO-STAR INT'L CO.,LTD

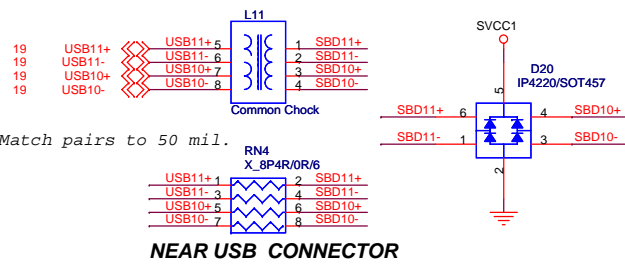
MS-7613

Size Custom Document Description **USB POWER** Rev 11

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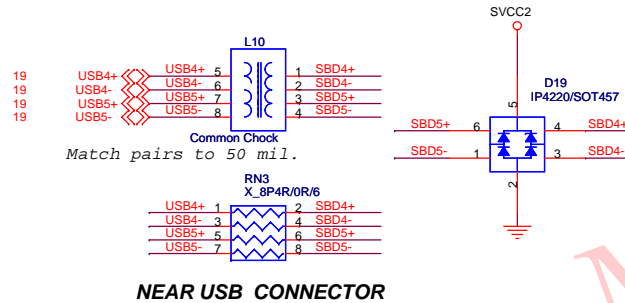
REAR PANEL USB CONNECTOR FOR USB PORT 10,11

Trace lengths must be less 12 inches



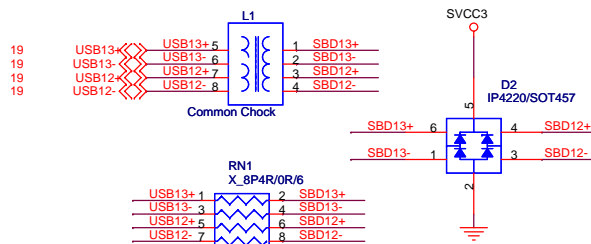
REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



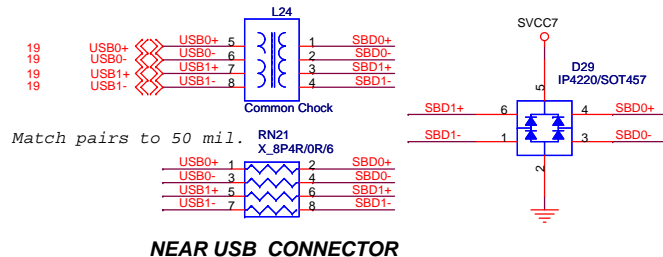
FRONT USB CONNECTOR FOR USB PORT 12,13

Trace lengths must be less 5 inches



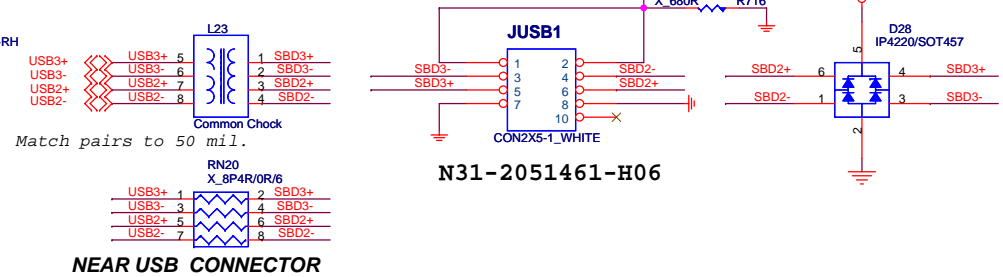
FRONT USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches



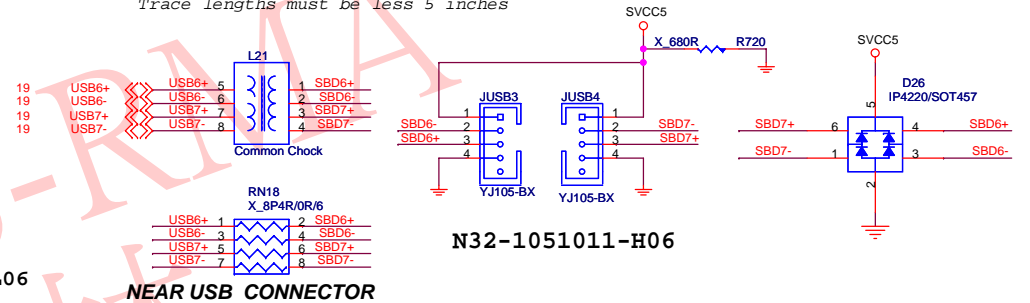
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 5 inches



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

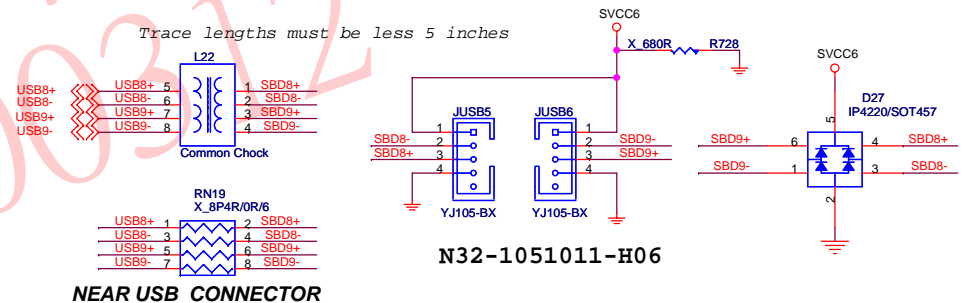
Trace lengths must be less 5 inches



NEAR USB CONNECTOR

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

N31-2051461-H06

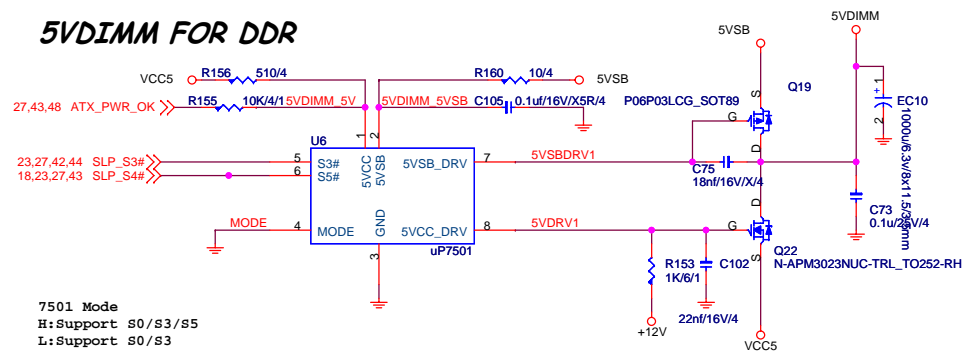


MICRO-STAR INT'L CO.,LTD

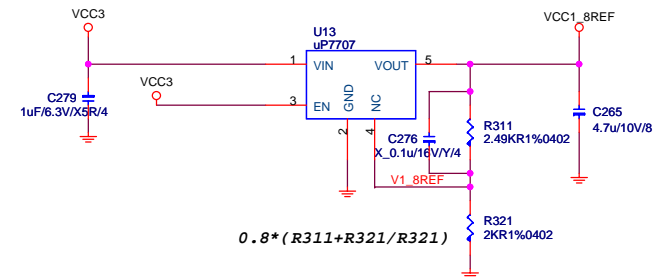
MS-7613

Size	Document Description	Rev
Custom	USB Conn.	11
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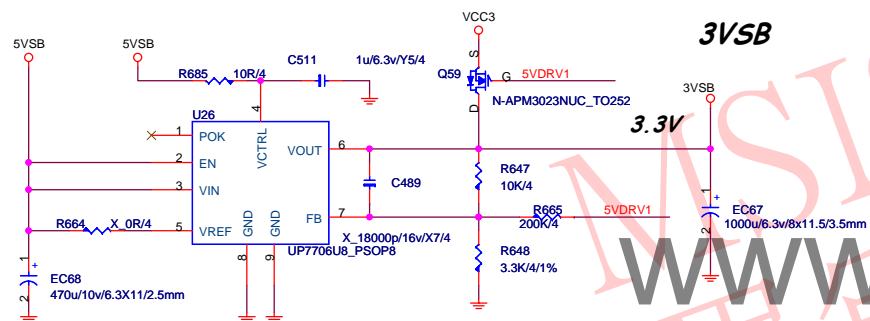
5VDIMM FOR DDR



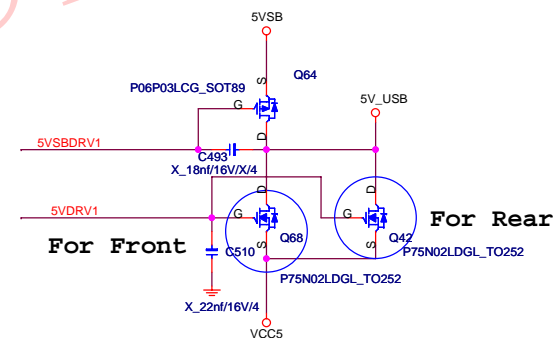
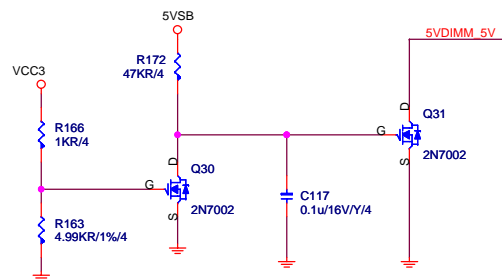
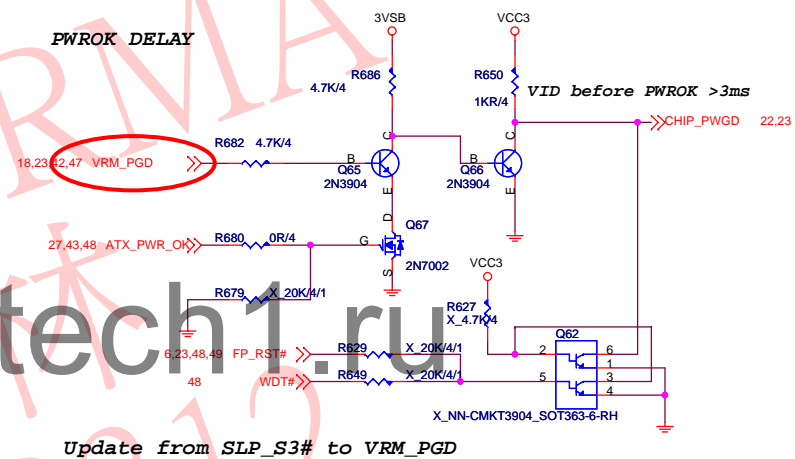
VCC1_8REF



3VSB



PWROK DELAY



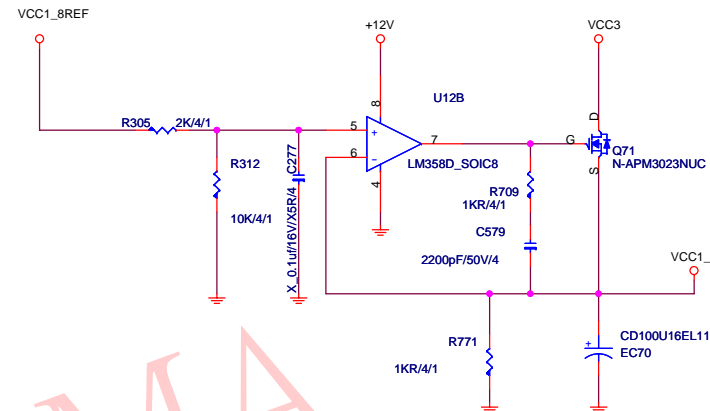
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MS-7613

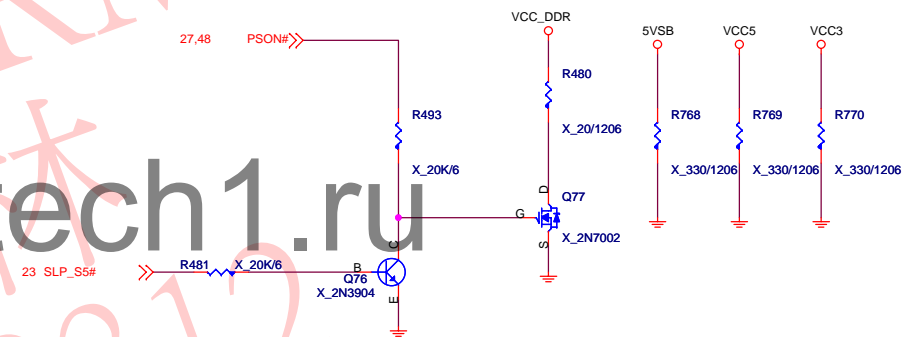
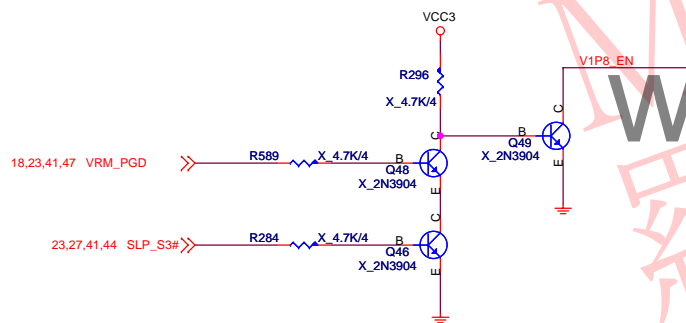
Size	Document Description
Custom	ACPI Controller 1

Rev	11
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cpuvtt & pch vore wait 1.8v



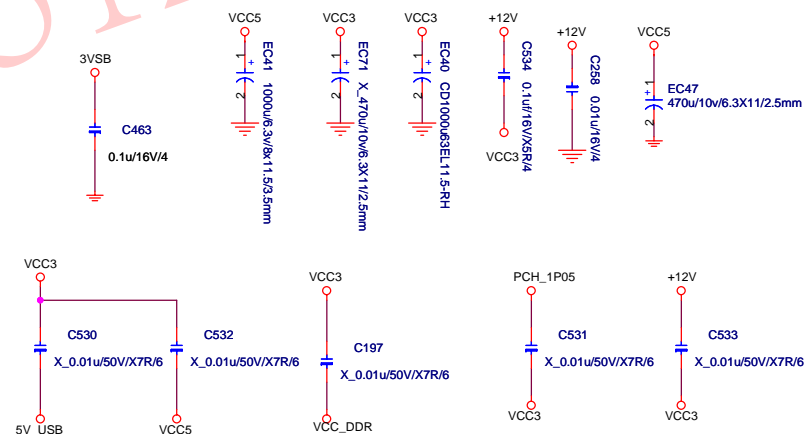
VCC_DDR

5VSB

3VSB

5V_USB

VCC5

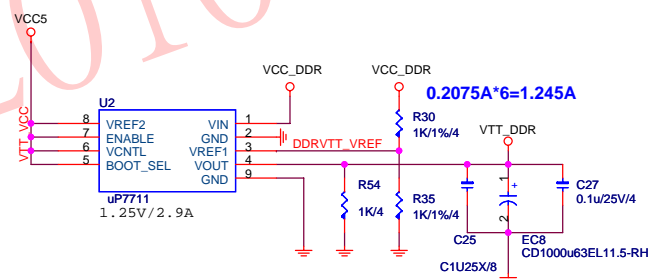
**MS-7613**

Size Custom	Document Description ACPI Controller 2	Rev 11
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20A

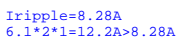


To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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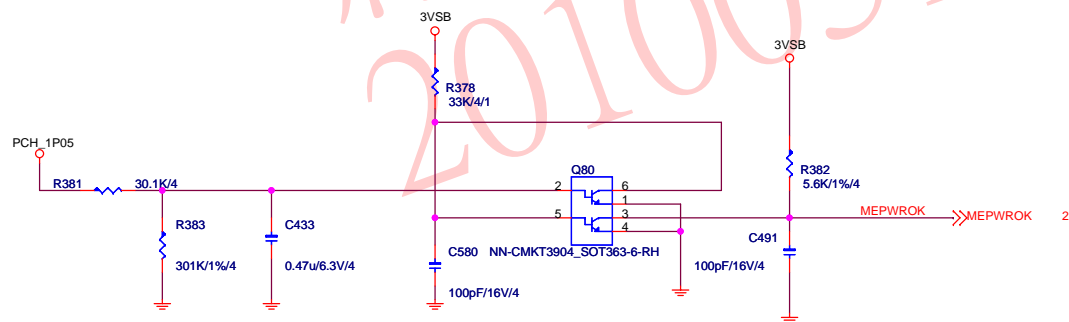
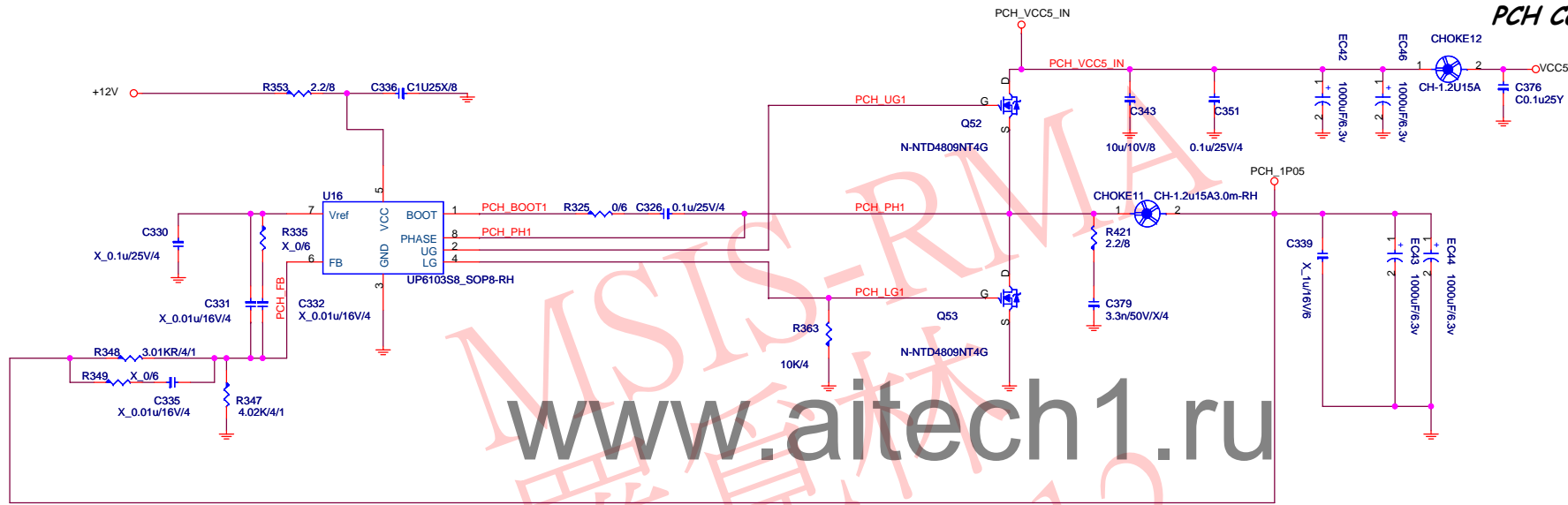
Size Custom	Document Description DDR POWER - UPI6103_1-Phase	Rev 11
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Size Custom	Document Description CPU_VTT - NCP1589A_1-Phase	Rev 11
Date: Tuesday, January 19, 2010	Sheet 44 of 53	

5.5A+2.5A(VCCME)=8A

PCH Core



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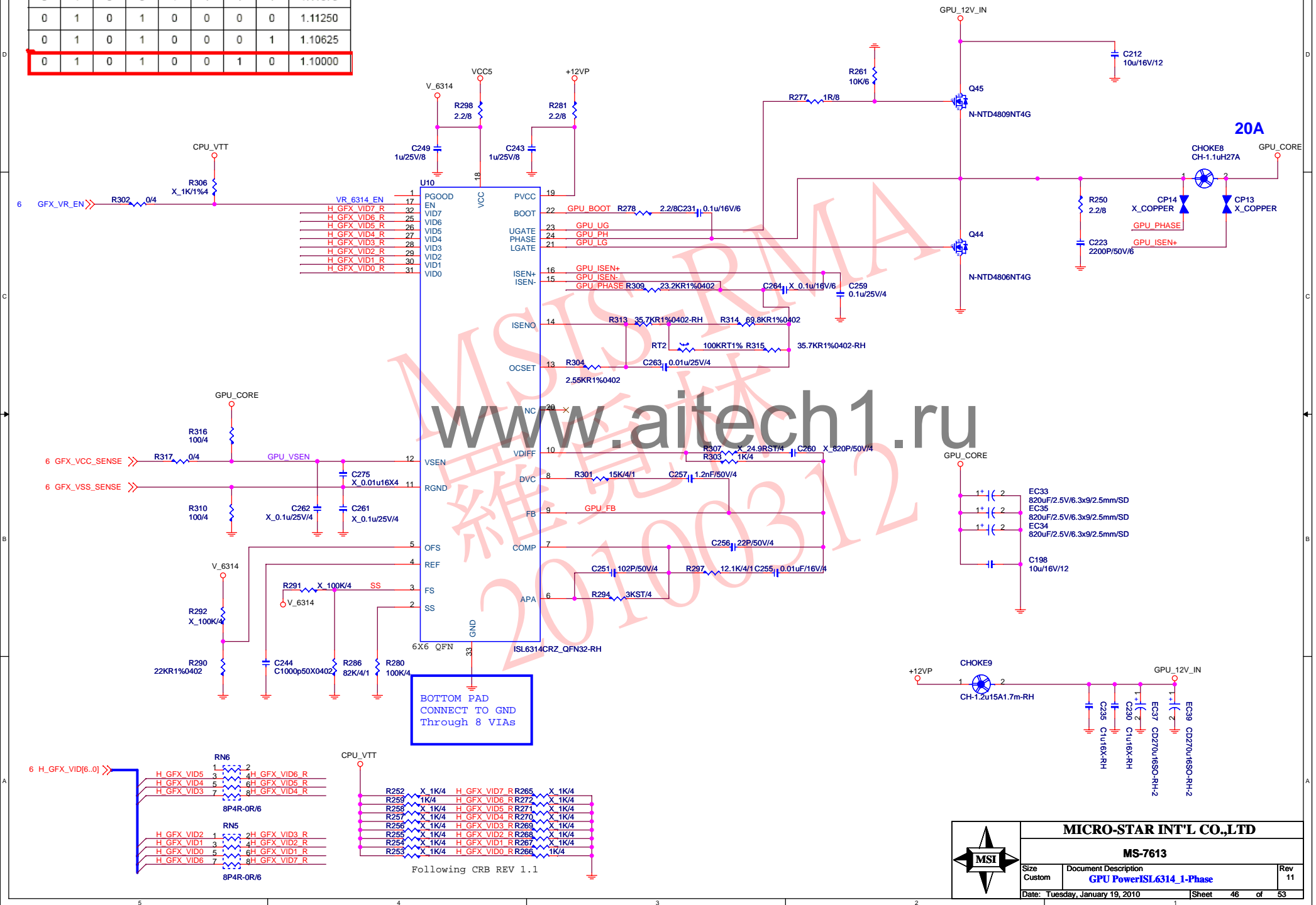
MS-7613

Size	Document Description	Rev
Custom	PCH POWER - UPI6103_1-Phase	11
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TABLE 2. VR11 VID 8 BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000

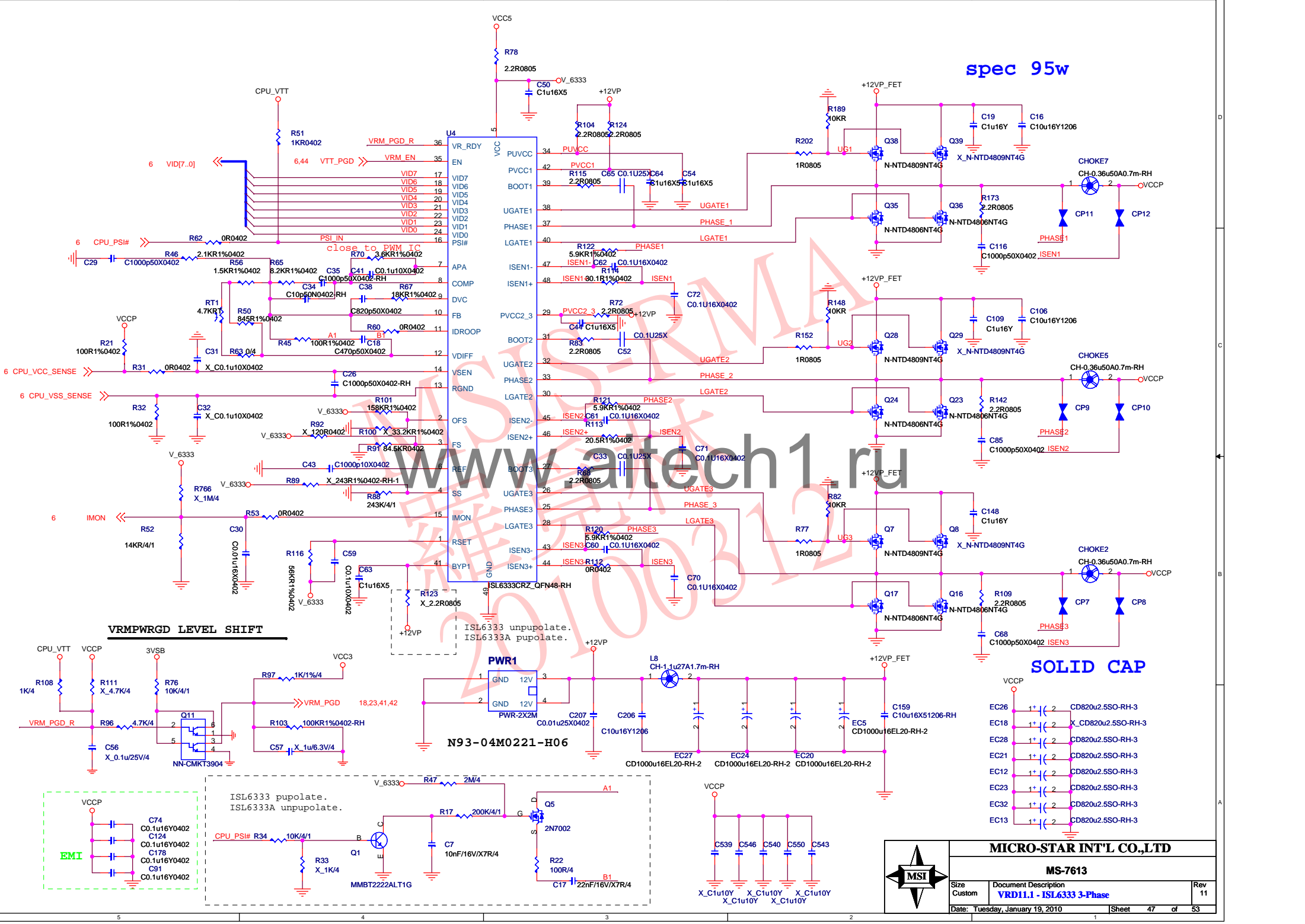
GPU_CORE 20A



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Size	Document Description	Rev
Custom	GPU PowerISL6314_1-Phase	11
Date:	Tuesday, January 19, 2010	Sheet 46 of 53



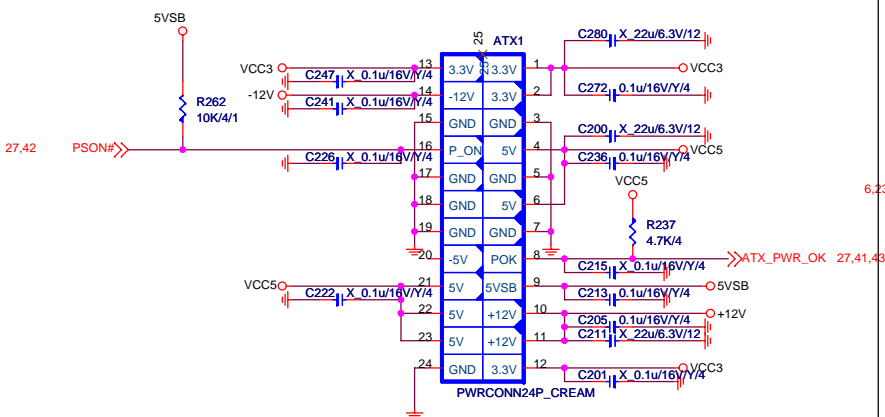
spec 95w

SOLID CAP

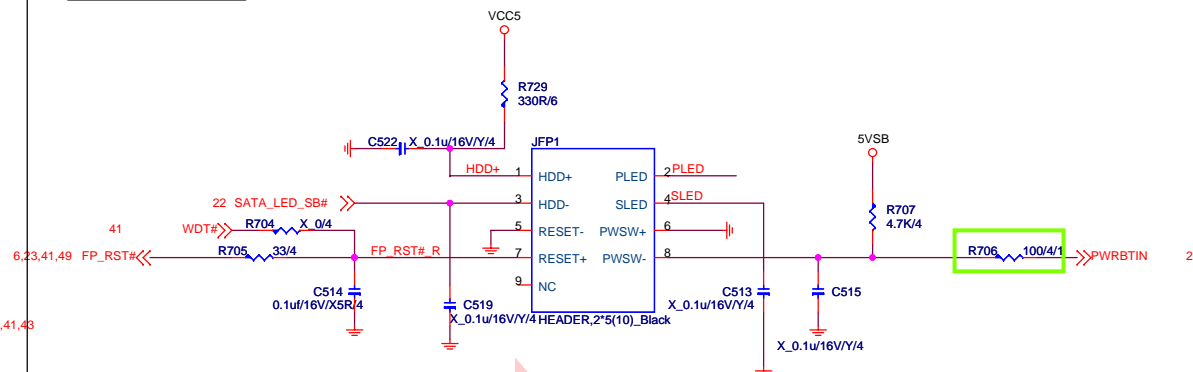


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MS-7613		
Size	Document Description	Rev
Custom	VRD11.1 - ISL6333 3-Phase	11
Date: Tuesday, January 19, 2010 Sheet 47 of 53		

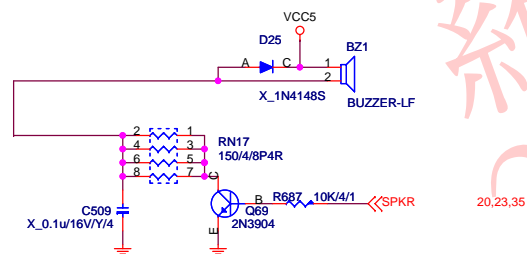
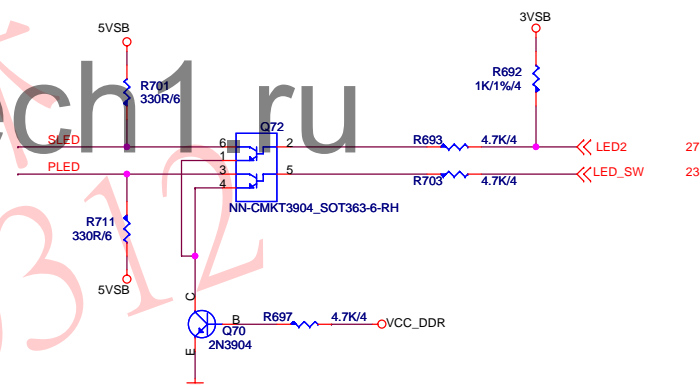
ATX POWER CONNECTOR



FRONT PANNEL



LED



	Single color LED		Dual color LED	
	LED2	LED_SW	LED2	LED_SW
S0	H	L	H	L
S1/S3	Blinking	L	L	H
S4/S5	L	L	L	L



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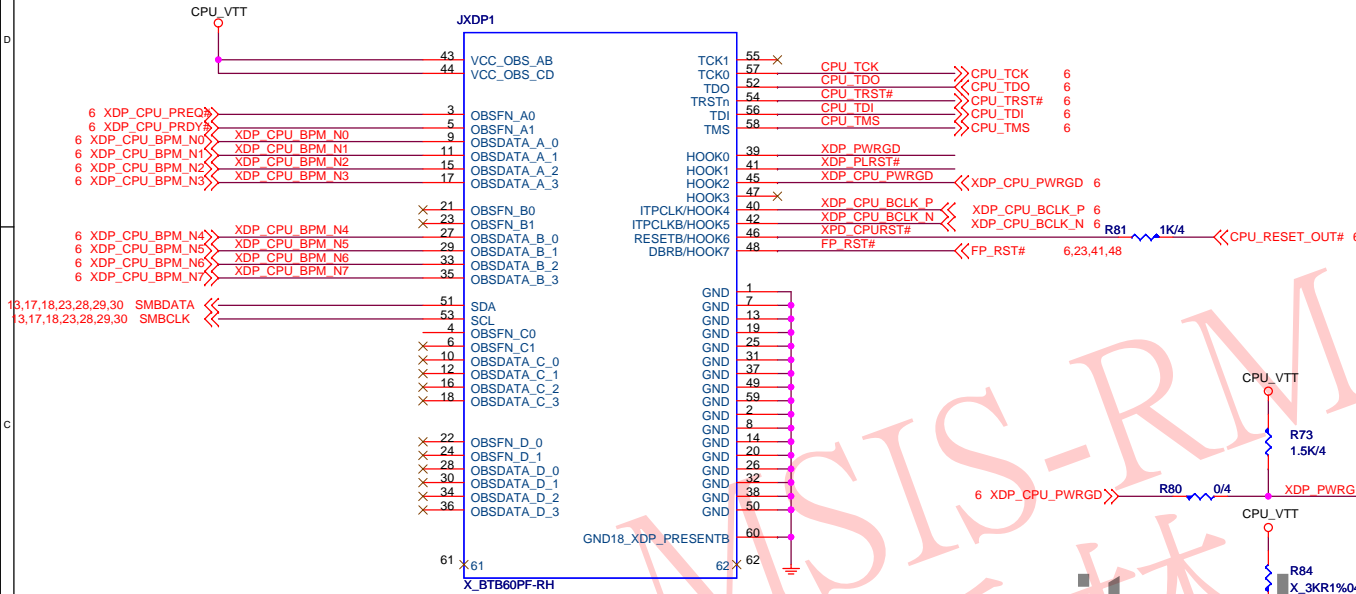
MS-7613

Size Custom Document Description
ATX PWR-Connector/LED

Rev 11

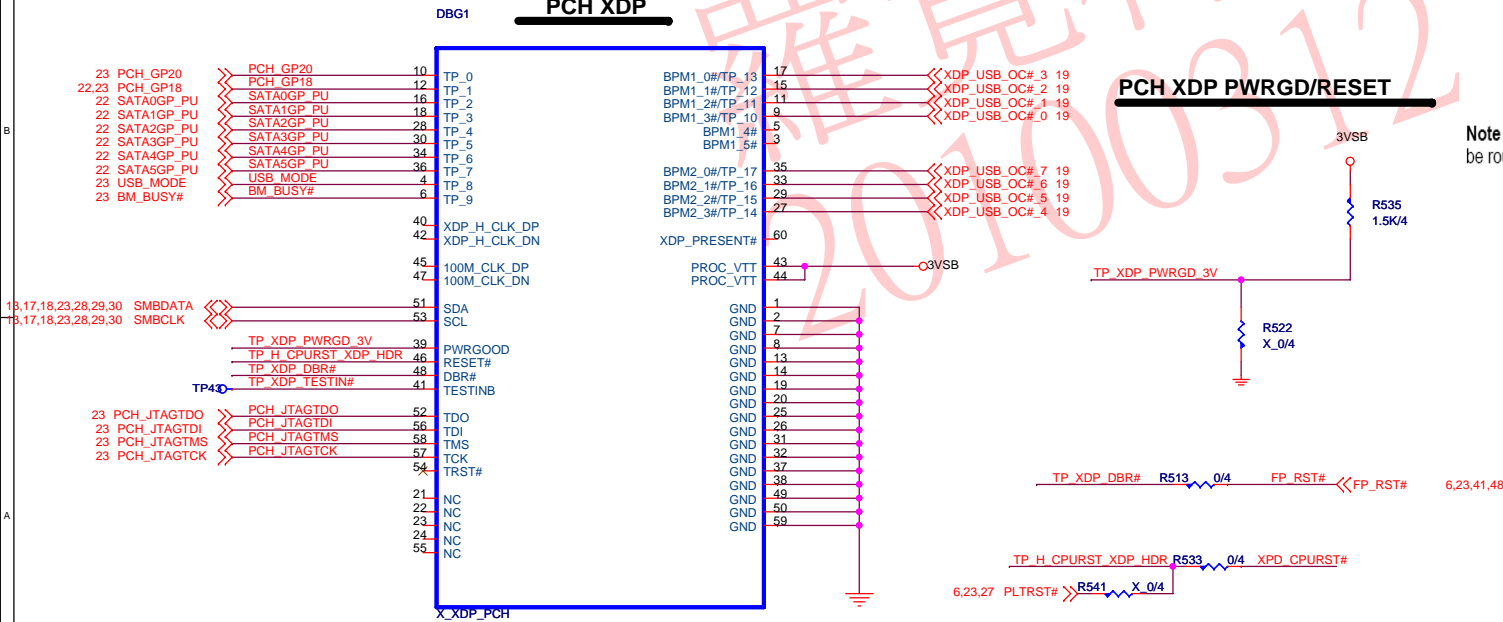
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Reserve debug port

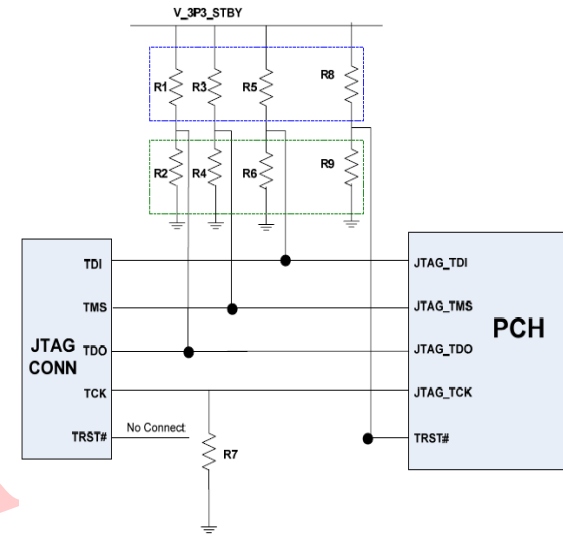


N5C-60F0040-S88

PCH XDP



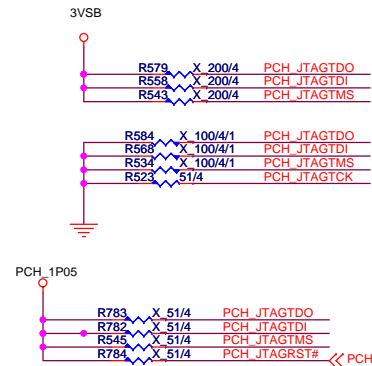
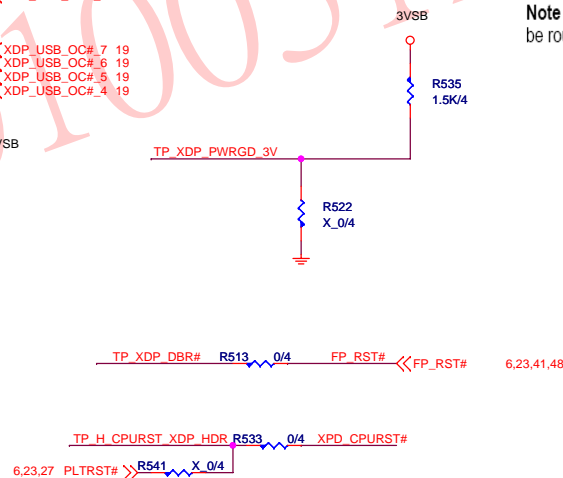
N5C-60F0040-S88



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stiff	200 Ohms	No Stuff
TDO	R2	No Stiff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
TMS	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
TDI	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable ¹	Not Applicable ¹
TRST#	R9	10K Ohms	Not Applicable ¹	Not Applicable ¹

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes.

PCH XDP PWRGD/RESET

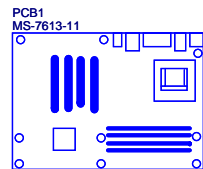


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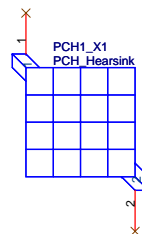
Size Custom	Document Description CPU/PCH XDP	Rev 11
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Date: Tuesday, January 19, 2010 Sheet 49 of 53

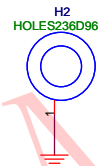
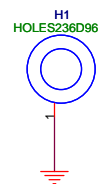
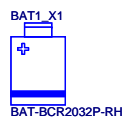
PCB



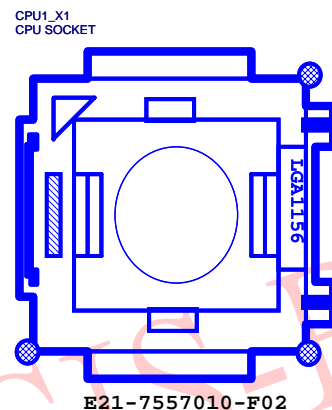
P30-0761311-G37



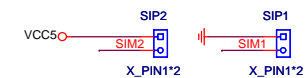
E31-0401634-K08



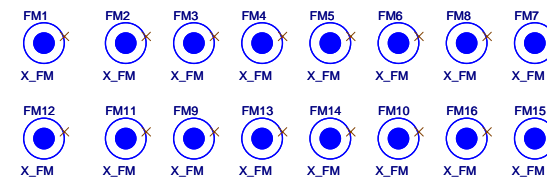
CPU SOCKET



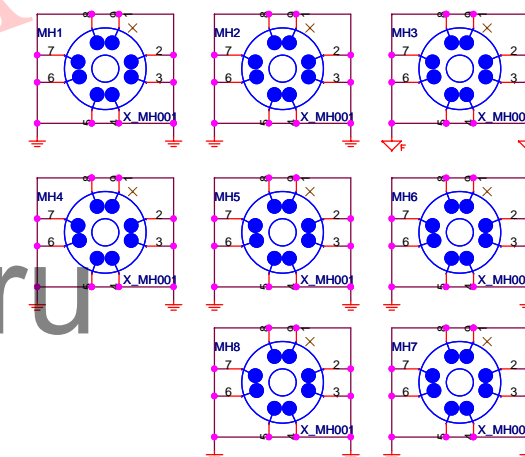
Simulation



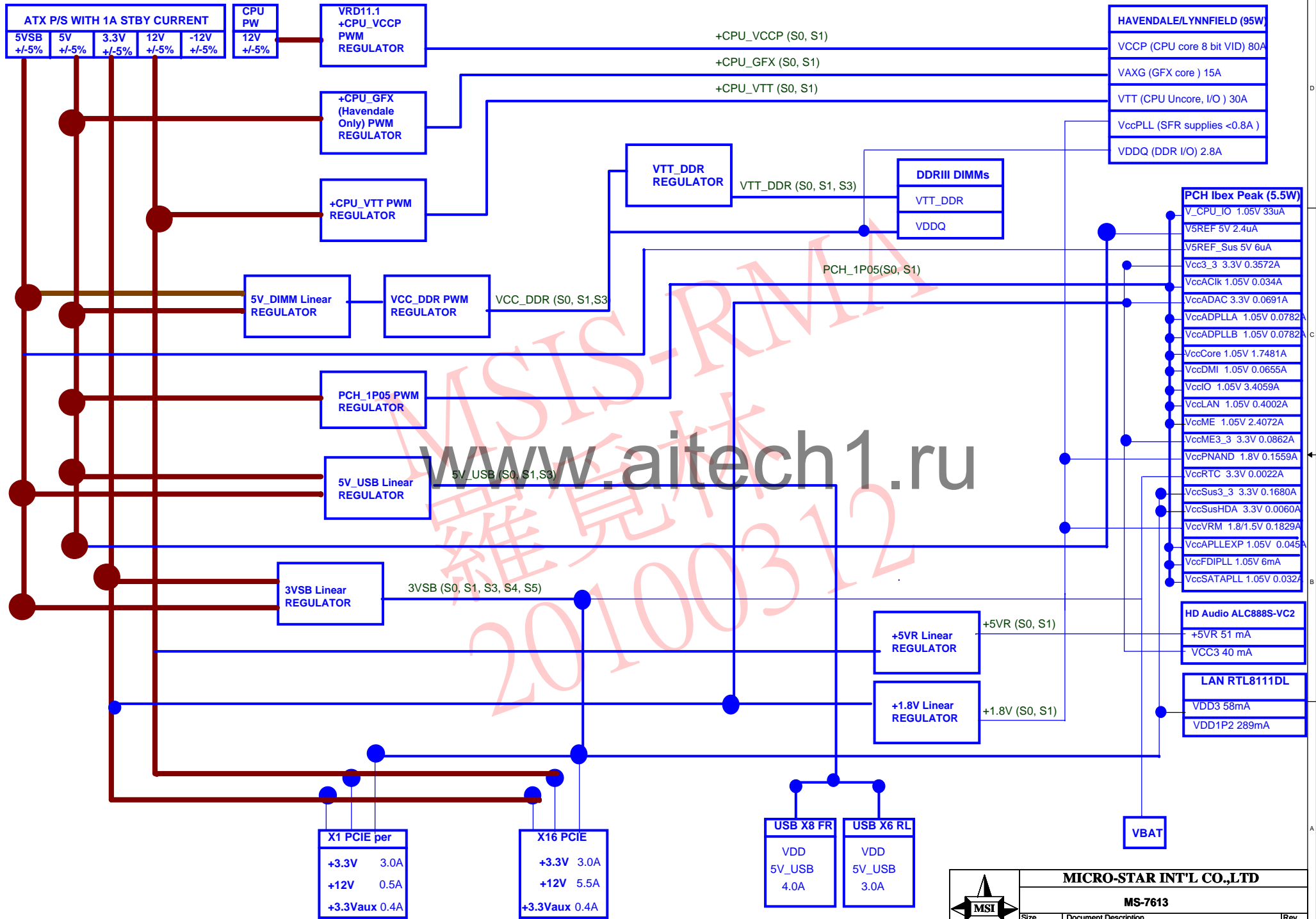
Optical Fiducial Marks-120



Mounting Holes



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Version 0A:

2009/03/16
Page 23: Populate R668 by Intel suggestion.
Page 23: Populate 100k ohm in R668 by Intel suggestion.
Page 23: Unpopulate R214 by Intel suggestion.

Version 0B:

2009/03/17
Page 35: Add internal amplifier circuit by HP requestion.
Page 34: Remove internal line-in circuit by HP requestion.
Page 6: Add CPU POC circuit following Design guide..
Page 47: Change R123 to 2.2ohm/0805 reserve for ISL6333A.
Page 39: Change USB port 0, 1 OC from OC#5 to OC#0 following Design guide.
Page 36: Change R143 and R140 from 100 ohm to 0 ohm by Intel suggestion.
Page 23: Pull-up GPIO57 to 3VSB by Intel suggestion.
Page 23: Unpopulate R603 by Intel suggestion.
Page 23: Pull-up SML0CLK and SML0DATA to 3VSB by Intel recommend.
Page 23: Pull-up SMBCLK and SMBDATA to 3VSB by Intel recommend.
Page 23: Swap HAD_SYNC and HAD_RST to match ball name.
Page 23: Connect PCH_JTAGRST# to a test point by Intel recommend.
Page 49: Connect SATA4GP to Pin 34 of the JTAG connector by Intel recommend.
Page 49: Connect Pin 41 of the JTAG connector to a test point by Intel recommend.
Page 49: Connect VCC of the JTAG connector to 3VSB by Intel recommend.
Page 23: Connect GIOP26 to control audio de-pop circuit.
Page 23: Use GPIO13 to switch audio Verb Table with internal amplifier or not.
Page 37: Reserve R512 for DVI level shifter eable control.
2009/03/19
Page 20: Change R539 and R546 from 39 ohm to 22 ohm by Intel recommend.
Page 27: Reserve R766 for RSMRST# timing control.
Page 23: Change GPIO45, GPIO46, GPIO47 pull-up well from VCC3 to 3VBS following schematic checklist.
Page 22: Connect SATA port4 to SATA5 connector by HP recommend.
Page 22: Connect SATA port2 to SATA3 connector by HP recommend.
Page 22: Use GPIO22, GPIO38, GPIO39, GPIO48 for MB_ID.
Page 32: Unpopulate C216 for EEPROM can not be programed issue.
2009/03/20
Page 42: Reserve discharge circuit.
Page 47: Connect IMON pin of VRD to ISENSE of CPU.
2009/03/23
Page 32: Unpopulate C209, C210, C214 to fix LAN LED wrong.
Page 42: Add R771 approve VCC1_5 whitout load.
2009/03/24
Page 22: Delete SATA5, SATA6 connector.
Page 22: Change SATA1 and SATA2 to right angle connector.
Page 15: Change C160 to 22uF/0805 and add a 22uF/0805 in C470.

2009/03/25
Page 23: Change R595 from 10k ohm to 1k ohm.
Page 23: Reserve R561 to pull-up FP_RST# to 3VSB.
Page 30: Add R813 and R814 to switch Mini-card support wake function or not.
Page 41: Change R650 from 4.7k ohm to 1k ohm for approving CHIP_PWGD signal level.
2009/03/26
Page 34: Move D24 to pin2 of U27.
Page 34: Change R681 from 309 ohm to 324 ohm.
Page 34: Connect D32 to 3VSB.
Page 30: Add Wireless LED (JWLED) by HP requirement.

2009/03/27

Power solution:

Page 47: Change R50 from 681 ohm to 931 ohm.
Page 47: Change R56 from 1.24k ohm to 1.33k ohm.
Page 47: Change R101 from 162k ohm to 255k ohm.
Page 47: Change C34 from 33 pF to 10 pF.
Page 47: Change C35 from 470 pF to 1000 pF.
Page 47: Change R65 from 16.5k ohm to 21k ohm.
Page 47: Change R70 from 5.1k ohm to 3k ohm.
Page 12: Populate C96 and C98.
Page 47: Populate 4700pF cap in C29 and 2.49k ohm resistor in R46.
Page 47: Change R52 from 13.3k ohm to 14.3k ohm.
Page 47: Change CHOKE2, CHOKE5 and CHOKE from 0.5uH to 0.36uH
Page 47: Populate EC32.
Page 47: Change R120, 121 and R122 from 6.19k ohm to 5.11k ohm.
Page 44: Change C6 from 0.015uF to 4700pF.
Page 44: Change R8 from 4.32k ohm to 4.12k ohm.
Page 44: Populate 820uF cap in EC78.
Page 44: Change EC76 from 100uF to 220uF and non-stuff EC77.
Page 44: Add a 820uF cap in EC79.

2009/03/30

Page 23: Change R642 from 4.75k ohm to 1.1k ohm.
and R641 from 12.1k ohm to 3k ohm following Intel MOW WW13 2009.
Page 27: Change R571 from 5.6k ohm to 5.9k ohm to meet RSMRST# falling spec.
and unpopulate C456 to meet RSMRST# falling spec.

2009/03/31

Page 20: Reserve C471, C479 and C483 for EMI.

2009/04/02

Page 26: Un-stuff R431 and R400.
Stuff R423, R401, R367, R475, R374 and R450 for using external LC filter.
Page 38: Connect Pin 1 of U1 to fix system fan always full on.
Page 48: Use GPIO31 to control power LED for LED turn red then green with dual color LED.
2009/04/06
Page 33: Reserve C485 for AZ_SDOUT.
2009/04/07
Page 34: Reserve Q78, Q79, R773, C475, R702, R773 for power saving in S5.
Page 43: Change R200 from 1.3k ohm to 1.33k ohm for DDR power quality.
Page 27: Add D36 and connect to ATX_PWR_OK for AC power lost last state function adnormal.

2009/04/09

Page 18: Change Clock gen from realtek RTM875N-606 to realtek RTM885N-932.
Page 44: Add D37 to fix CPU_VTT leakage in S3 state.

Version 0C:

2009/04/21

Page 23: Add C365 to fix sometime the system auto wake when insert PCIE device.
Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.
Page 23: Use GPIO44 to control onboard LAN power.

2009/04/27

Page 28: Reserve C412 for PCIE slot power.
Page 34: Reserve C419 for audio power.



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Version 0C:

2009/04/21

Page 23: Reserve C365 to fix sometime the system auto wake when insert PCIE device.

Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.

Page 23: Use GPIO44 to control onboard LAN power.

2009/04/27

Page 28: Add C412 for PCIE slot power.

Page 34: Reserve C419 for audio power.

2009/05/06

Page 40: Leave pin10 of JUSB1 and JUSB2 NC for some card reader work abnormal.

Page 41: Change EC67 to 1000uF for 3VSB power quality.

Page 37: Swap DVI_TXD2+ and DVI_TXD2-.

2009/05/07

Power Solution:

Page 12: Unpopulate C146, C139, C181

Page 12: Unpopulate C142, C155, C168, C171, C179, C176, C167, C145

Page 44: Change EC76 from 220uF to 100uF.

Page 44: Change C6 from 4700pF to 1000pF.

Page 47: Change R101 from 255k ohm to 158k ohm.

Page 47: Change C18 from 680 pF to 470pF.

Page 47: Change R70 from 3k ohm to 2.74k ohm.

Page 47: Change R120, R121 and R122 from 5.1k ohm to 5.9k ohm.

Page 47: Change C29 from 4700 pF to 1000pF.

Page 47: Change R46 from 2.49k ohm to 2.1k ohm.

Page 47: Change R45 from 750 ohm to 100 ohm.

Page 47: Change R65 from 2.1k ohm to 8.2k ohm.

Page 47: Change C35 from 1000 pF to 3300pF.

Page 47: Change R52 from 14.3k ohm to 14k ohm.

Page 47: Change R56 from 1.33k ohm to 1.4k ohm.

Page 46: Change R290 from 9.1k ohm to 15.4k ohm.

Page 46: Change R309 from 19.6k ohm to 23.7k ohm.

Page 46: Change R286 from 100k ohm to 82k ohm.

2009/05/11

Page 18: Change clock gen from RTM885N-932 to Seligo SLG8SP585

Page 27: Change R571 from 5.9K ohm to 5.6K ohm for meet RSMRST# falling time.

Page 12: Populate 0 ohm in C186 following WW16 MoW

(Discrete graphic only support, VAXG tie to GND)

Page 11: Populate R293, R299 following WW18 MoW

Page 30: Connect LED_WLED to pin4 of JWLED for meet LED cable define.

Page 22: Change SATA1 and SATA2 connector type to DIP.

2009/05/18

Page 23: Change C495 and C500 from 10pF to 18pF.

Page 13, 15: Change C137 and C161 from 0.1uF to 2.2uF to improve Vref_CA power.

Page 30: Reserve R780 for mini card.

Page 30: Connect R813 to 3VSB_SLOT.

Page 21: Add R375 and R376 for support two TL-399.

2009/05/26

Page 23: Populate R619 to fix TV tuner card can't be detected when system restart.

2009/06/16

Power Solution:

Page 46: Un-stuff R33.

Page 46: Change R50 from 931 ohm to 845 ohm.

Page 46: Change R56 from 1.4K ohm to 1.5K ohm.

Page 46: Change R70 from 2.74K ohm to 3.6K ohm.

Page 46: Change C35 from 3300 pF to 1000 pF.

Page 46: Stuff 1000 pF in C26.

Page 44: Change R6 from 69.8K ohm to 59K ohm.

2009/06/22

Page 24: Un-stuff C560

Page 24: Change C557 to 0 ohm.

2009/06/25

Page 39: Change R216,R212,R40,R733,R715,R719,R732 from 220 ohm to 10K ohm.

Page 39: Change R217,R213,R59,R723,R710,R708,R723 from 330 ohm to 15K ohm.

Version 0D:

2009/06/22

Page 45: Add MEPWRGD circuit.

2009/06/25

Page 23: Add JME1 header.

2009/06/26

Page 37: Reserve C581 for EMI.

2009/06/30

Page 20: Add R393 and R395.

2009/07/02

Page 42: Reserver C582 and C583 for EMI.

Page 49: Reserve R545,R782,R783 and R784.

2009/07/09

Page 49: Un-stuff R579,R558,R543,R584,R568,R534.

2009/07/14

Power Solution:

Page 44: Un-stuff R16.

Page 44: Stuff 4.12k ohm in R7.

Page 44: Stuff 13k ohm in R18.

Page 44: Stuff 0.01uF in C13.

Page 46: Change C244 from 10nf to 1nf

Page 46: Un-stuff R290.

Page 46: Change R301 from 15k ohm to 9.1k ohm

2009/07/21

Page 32: stuff 1000pf cap in C209,C210,C214,C216,C244 for EMI.

Page 42: stuff 47pf cap in C93,C94,C95 for EMI.

2009/07/29

Page 22: Change MB ID to 1010.

Page 27: Change R565 from 4.7K to 10K ohm.

Version 10:

2009/10/05

Page 30: Un-stuff ONFI slot.

Page 37: Un-stuff R171 to change DVI Vswing to 600mV.

Page 46: Stuff 22K ohm in R171 for power solution.


Page 20: Change PCH PN to B01-BD82H45-IX6

Version 11:

2010/01/11

Page 30: Connect Pin 5 of RN10 to VCC3 for PCI_E2 slot download files slowly from PXE server with LAN card.

Page 37: Connect DVI connector power pin to DVI_PWR_SV for safety.

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